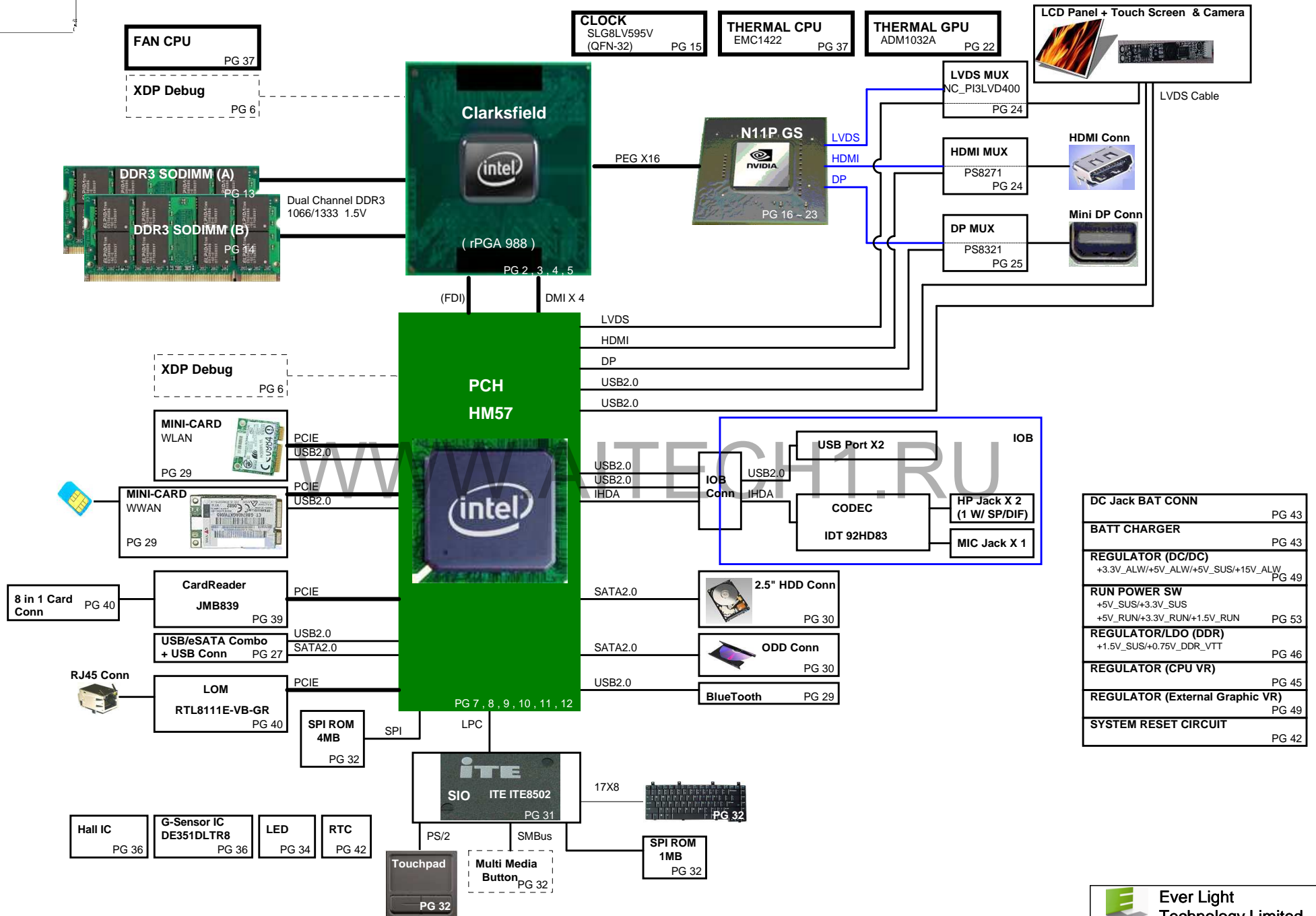
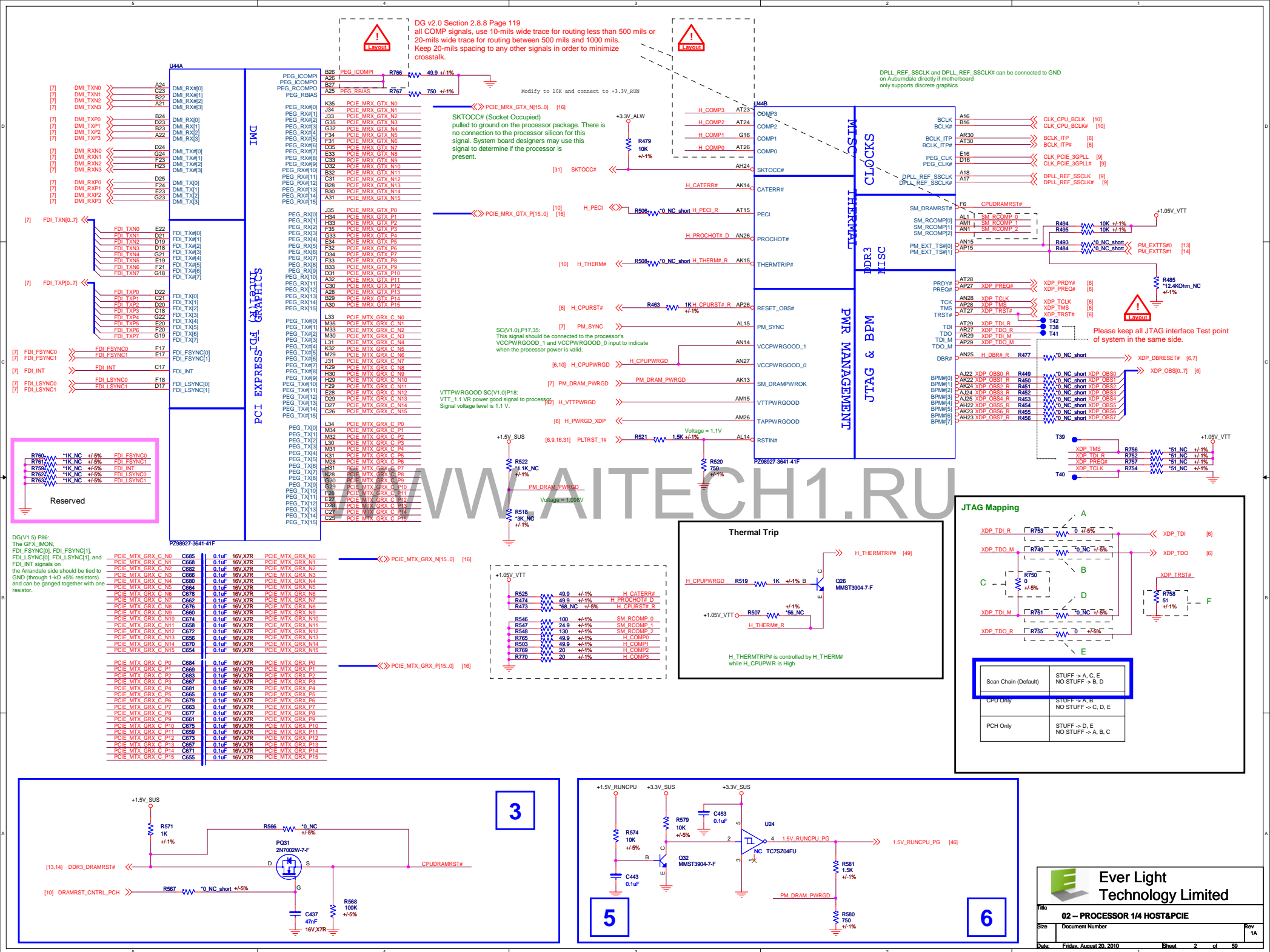


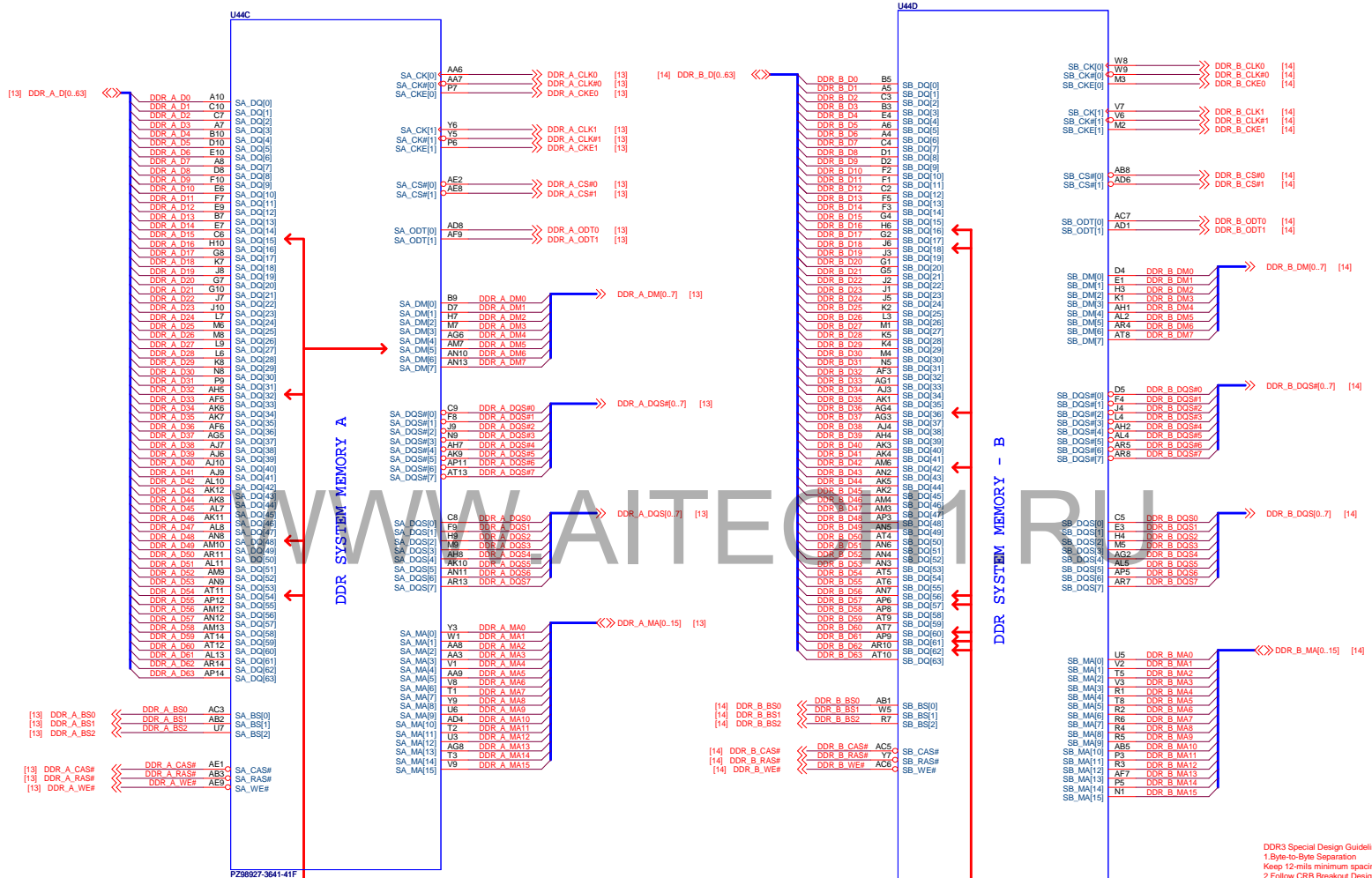
# Nichols 14" Calpella DIS Block Diagram



DC Jack BAT CONN	PG 43
BATT CHARGER	PG 43
REGULATOR (DC/DC)	PG 49
RUN POWER SW	PG 53
REGULATOR/LDO (DDR)	PG 46
REGULATOR (CPU VR)	PG 45
REGULATOR (External Graphic VR)	PG 49
SYSTEM RESET CIRCUIT	PG 42



# ARRANDALE PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

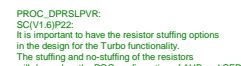
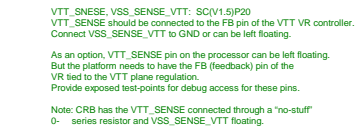
DDR3 Special Design Guideline, DG v1.6 Page 105.

DDR3 Special Design Guideline, DG v1.6 Page 105.  
1. Byte-to-Byte Separation  
Keep 12-mils minimum spacing between different byte lanes  
2. Follow CRB Breakout Designs or Further Optimize it.  
Try to reduce breakout length, even for signals buried deep in the pinmap, and use maximum 2-track routing in order to minimize crosstalk between byte lanes.  
3. Additional GND Stitching Vias in the SO-DIMM Connector Area.  
In the SO-DIMM connector area, many signal transitions happen between layers, and Intel strongly recommend improving GND stitching via locations in order to achieve better return current flow. Try to break-in signals and GND vias from the same side of the SO-DIMM connector if possible. For each signal via, it's preferable to have a GND via within 100 mils. The GND via can be shared with other signals close by.  
4. Special design rules for certain data signals  
In addition to the routing guidelines described in Section 2.5.3.4, Intel introduces a special design rule, for a few of the data lines listed in table below. This is to compensate for larger-than-average crosstalk at the package, socket and motherboard breakout. All of these signals should have a minimum of 12-mil spacing with all signals, including Data signals.

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03 -- PROCESSOR 2/4(DDR)			Rev 1A
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## U44F




- CRB(V1.6) Page 60:
  - uses 1K pull-up and pull-down resistors
  - CRB default setting is "1"

**PSI#:**  
PSI# signal is provided by CPU to indicate maximum possible core currents at given CPU frequency (voltage). PSI# can be asserted or deasserted during active mode execution. Processor will not draw significant amount of current while in very low power state, and will have PSI# asserted.

Note: It is important to have the resistor stuffing options in the design for the Turbo functionality. The stuffing and no-stuffing of the resistor will depend on the POC configuration of ARD and CFD.  
Default setting can be "0"

CRB(V1.6) Page 60:  
uses 1K pull-up and pull-down resistors  
CRB default setting is "0"

 18-mil width, and should use differential routing with 7-mil separation. Signals must have equal trace length within 25 mils and are to be routed using external layer and GND referencing (no split plane referencing). VSS, SENSE, VCC, SENSE are to use 25-mils separation from any other signal or rail.

GFX\_VR\_EN  
 R471  
 470  
 +/-5%

GFX DPRSLPVR  
 R768  
 4.7K\_NC  
 +/-5%

11/11/2019

C411 0.1uF, 16V, X7R

C405 22pF, 50V, NPO

C410 22pF, 50V, NPO

5V\_SUS                      +1.5V\_RUNCPU

A circuit diagram showing a 470pF capacitor (C426) connected to a 50V source and a 0.5% resistor. The capacitor is labeled "C426 470pF\_NC 50V\_X7R". The resistor is labeled "0.5%". The circuit is connected to a ground symbol.

712  
2uF  
V,X6S

SUS +1.5V\_RUNCPU

C430 0.1uF  
16V,X7R

C429 0.1uF  
16V,X7R

C428 0.1uF  
16V,X7R

stitching Via.

\_\_\_\_\_

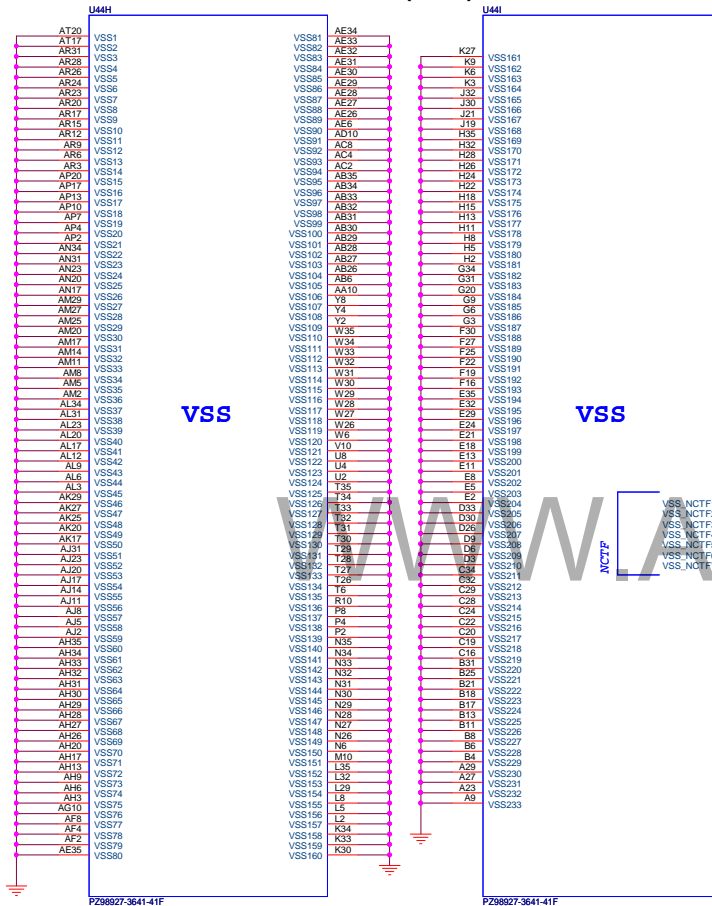
Rev  
1A

Sheet 4 of 59

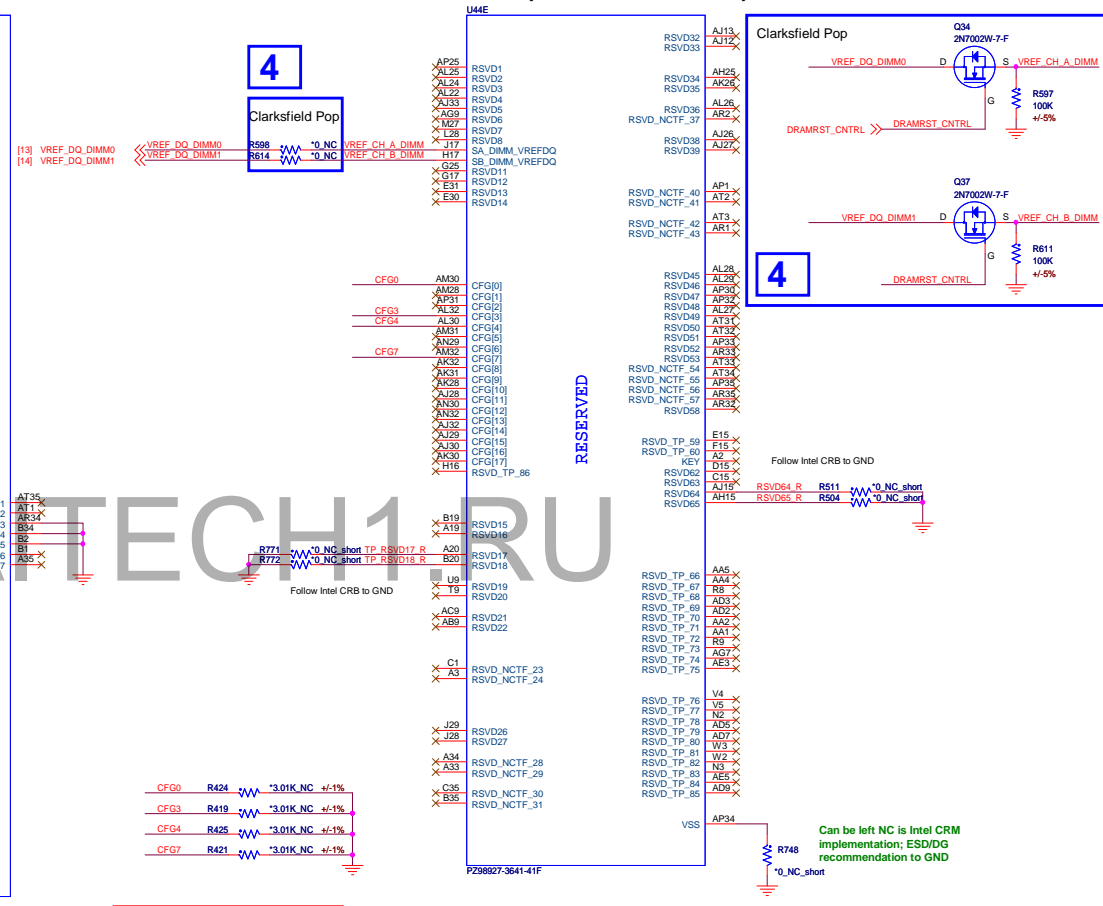


M3

## ARRANDALE PROCESSOR (GND)



## ARRANDALE PROCESSOR( RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

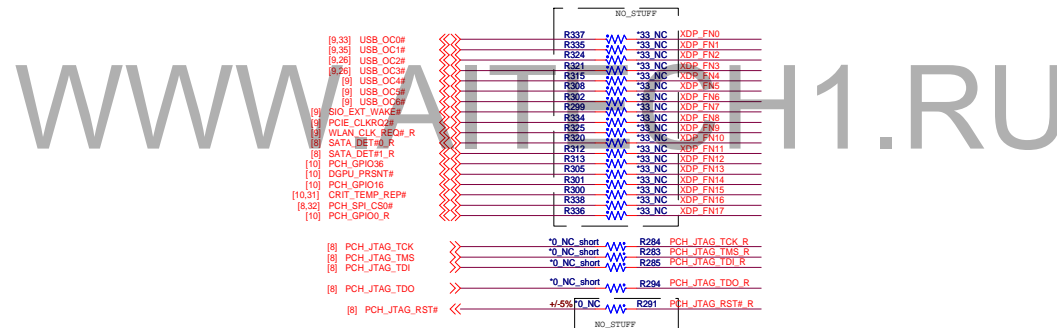
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port (Default Value)	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG (Default Value)	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation (Default Value)	Lane Numbers Reversed

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05 -- PROCESSOR 4/4(GND)

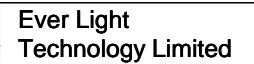
Size Document Number Rev 1A

Date: Friday, August 20, 2010 Sheet 5 of 59

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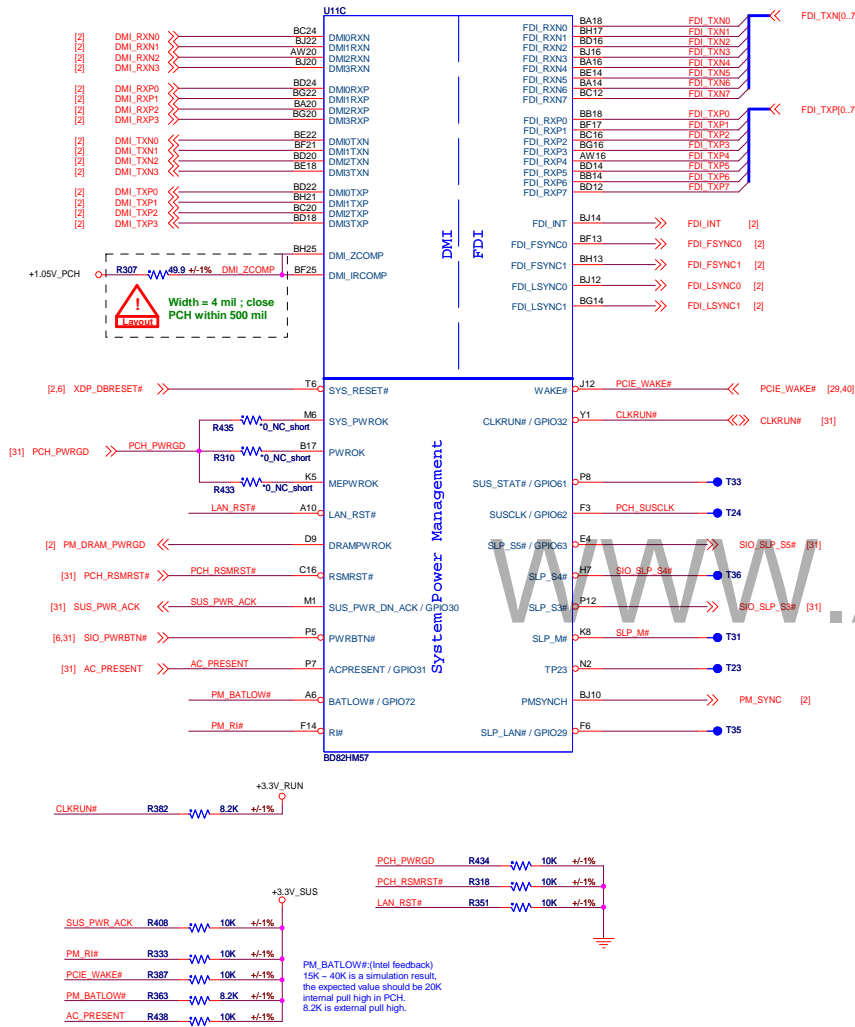
The schematic shows the connector pinout with the following connections:

- Power and Ground:**
  - +3.3V, RUN to pins 2 and 7.
  - GND0 to pin 1.
  - GND1 to pin 2.
  - GND2 to pin 9.
  - GND3 to pin 10.
  - GND4 to pin 51.
  - GND5 to pin 52.
  - GND6 to pin 59.
  - GND7 to pin 20.
  - GND8 to pin 27.
  - GND9 to pin 28.
  - GND10 to pin 33.
  - GND11 to pin 34.
  - GND12 to pin 42.
  - GND13 to pin 43.
  - GND14 to pin 51.
  - GND15 to pin 52.
  - GND16 to pin 59.
  - GND17 to pin 60.
- IO Signals:**
  - OBSPFN\_A0 to pin 3.
  - OBSPFN\_A1 to pin 5.
  - OBSPFN\_B0 to pin 23.
  - OBSPFN\_B1 to pin 25.
  - OBSPFN\_D0 to pin 22.
  - OBSPFN\_D1 to pin 24.
  - OBSPFN\_D2 to pin 36.
  - OBSPFN\_D3 to pin 38.
  - OBSPFN\_D4 to pin 40.
  - OBSPFN\_D5 to pin 41.
  - OBSPFN\_D6 to pin 43.
  - OBSPFN\_D7 to pin 44.
  - OBSPFN\_D8 to pin 45.
  - OBSPFN\_D9 to pin 46.
  - OBSPFN\_D10 to pin 47.
  - OBSPFN\_D11 to pin 48.
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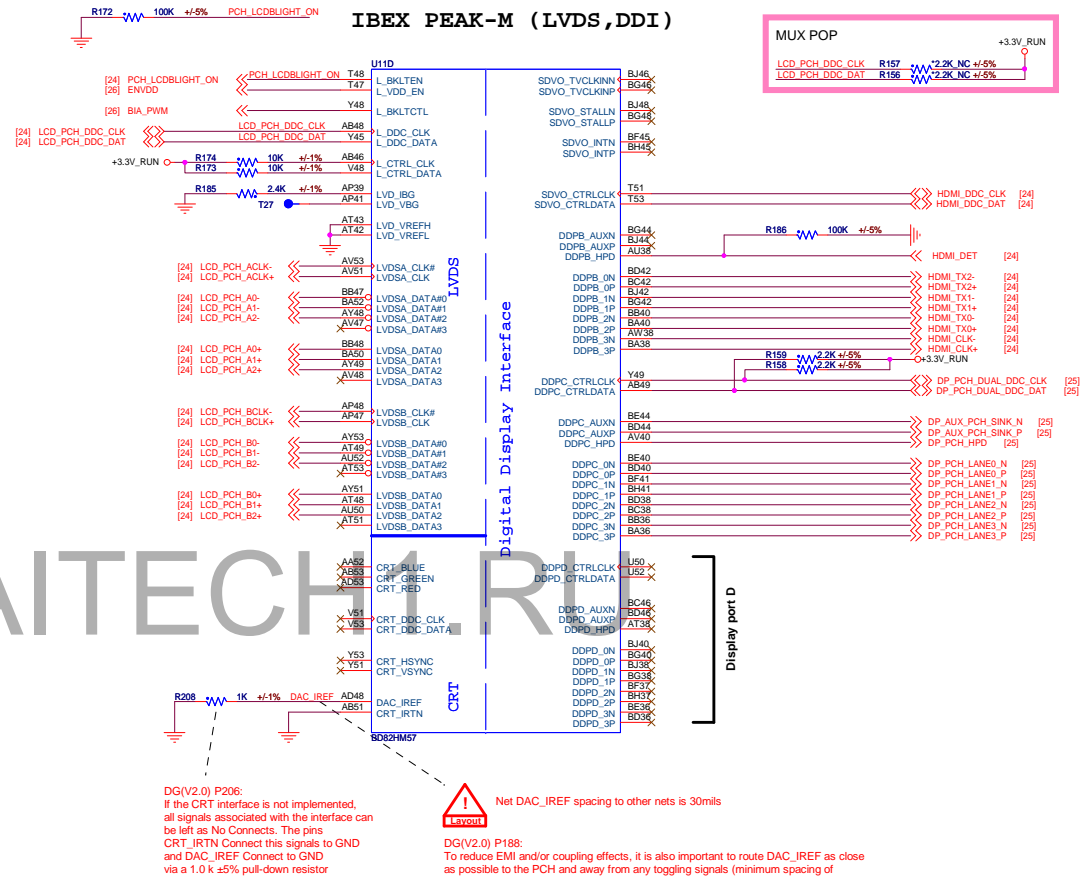


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## IBEX PEAK-M (DMI,FDI,GPIO)



## IBEX PEAK-M (LVDS,DDI)



**DG(V2.0) P206:**  
If the CRT interface is not implemented, all signals associated with the interface can be left as No Connects. The pins CRT\_IRTN Connect this signals to GND and DAC\_IREF Connect to GND via a 1.0 k  $\pm$ 5% pull-down resistor

 Net DAC\_IREF spacing to other nets is 30mils

**DG(V2.0) P188:**  
To reduce EMI and/or coupling effects, it is also important to route DAC\_IREF as close as possible to the PCH and away from any toggling signals (minimum spacing of 30 mils or 0.762 mm). No specific trace width or trace impedance is required for this signal. Routing DAC\_IREF close to any toggling signals distorts the display. Distortion may vary from blinking/burning dots, rippling lines, wavy lines, etc

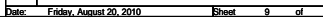
DG(V2.0) P188:  
If the CRT interface is implemented,  
DAC\_IREF Connect to GND  
via a 1.0 k  $\pm 0.5\%$  pull-down resistor

IBEX PEAK-M (HDA,JTAG,SATA)



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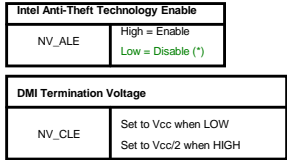
## IBEX PEAK-M (PCI-E,SMBUS,CLK)





Pinout diagram for the AITECH1.RU module. The diagram shows a 16-pin connector with the following labels and connections:


- Left Section (NCTF):**
  - A4: VSS.NCTF.1
  - A49: VSS.NCTF.2
  - A53: VSS.NCTF.3
  - A50: VSS.NCTF.4
  - A52: VSS.NCTF.5
  - A58: VSS.NCTF.6
  - B2: VSS.NCTF.7
- Right Section (R,SYD):**
  - N18: TP10
  - J24: TP11
  - AK42: TP12
  - M32: TP13
  - TP14



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Integrated Clock Chip Enable	
(Reserve to validate for future platforms)	
RSV_WOL_EN	Enable when sampled low Disable when sampled high

SV_SET_UP	1-X High = Strong (Default)
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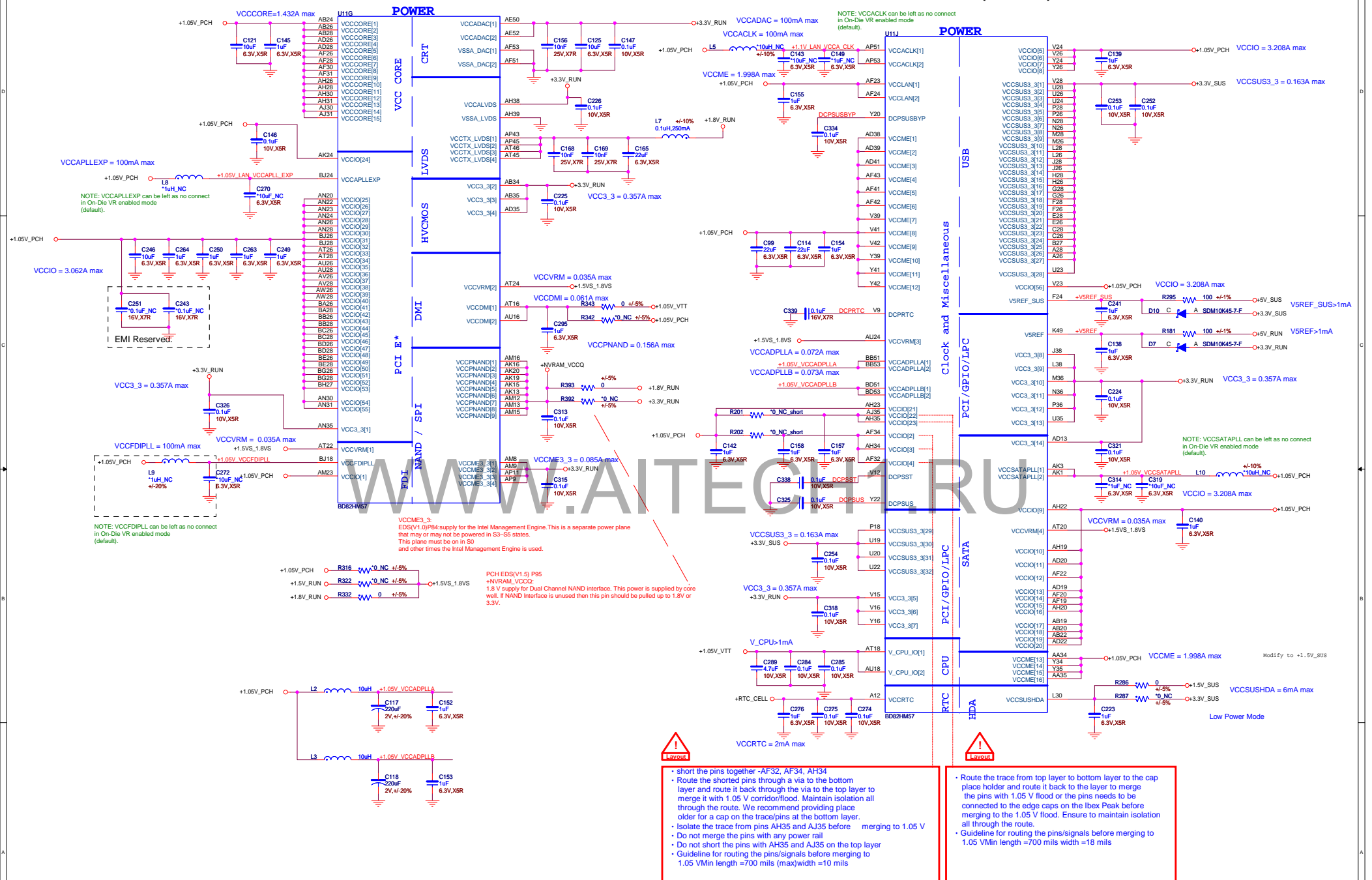
**10 – PCH 4/G (GPIO)**

Size Document Number Rev 1A

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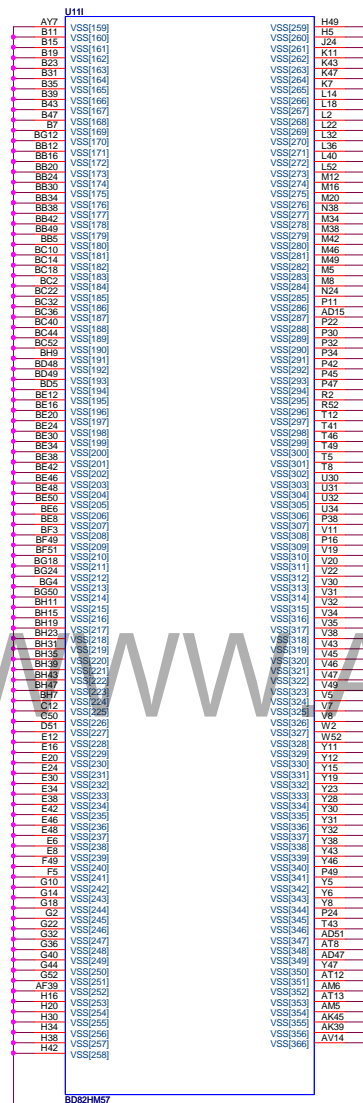
### IBEX PEAK-M (POWER)



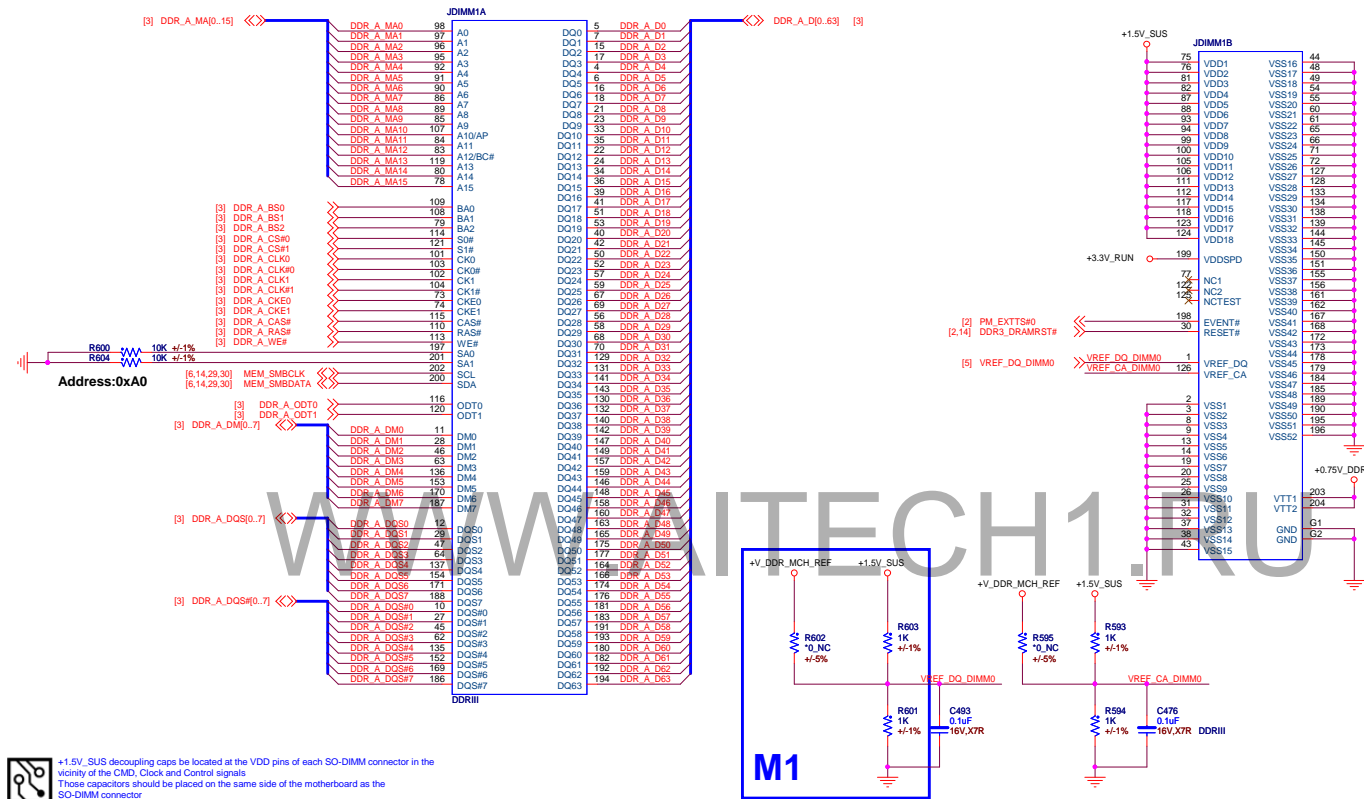
Ibex Peak DisplayPort interface may violate the Non ISI Jitter Measurements and Total Jitter Measurements tests due to the power delivery noise on specific VccIO pins.  
This fix would also applicable to HDMI 1080P 60Hz Deep color mode.  
Please see Intel Doc No.430877 Intel®5 Series Chipset (Ibex Peak) DisplayPort\* Jitter Technical Advisory



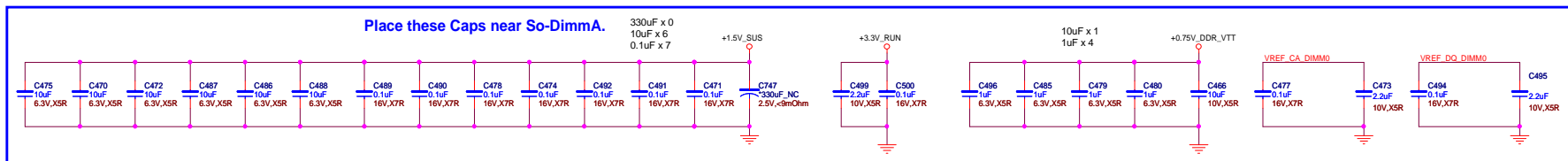
Title		
11 -- PCH 5/6 (POWER)		
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DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



+1.5V\_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals. These capacitors should be placed on the same side of the motherboard as the SO-DIMM connector

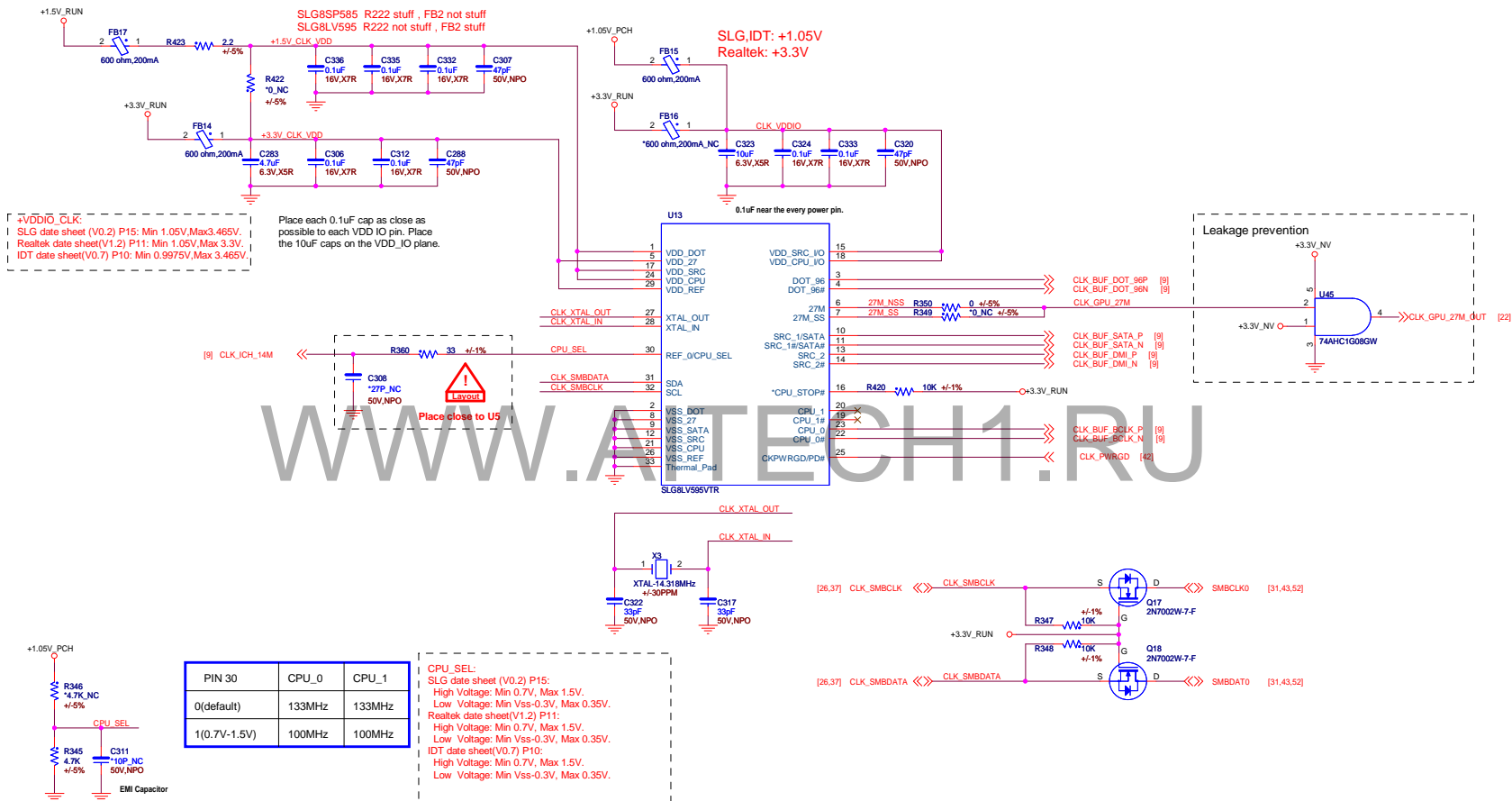


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13 -- SODIMMA-204P		
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Frame Buffer Interface

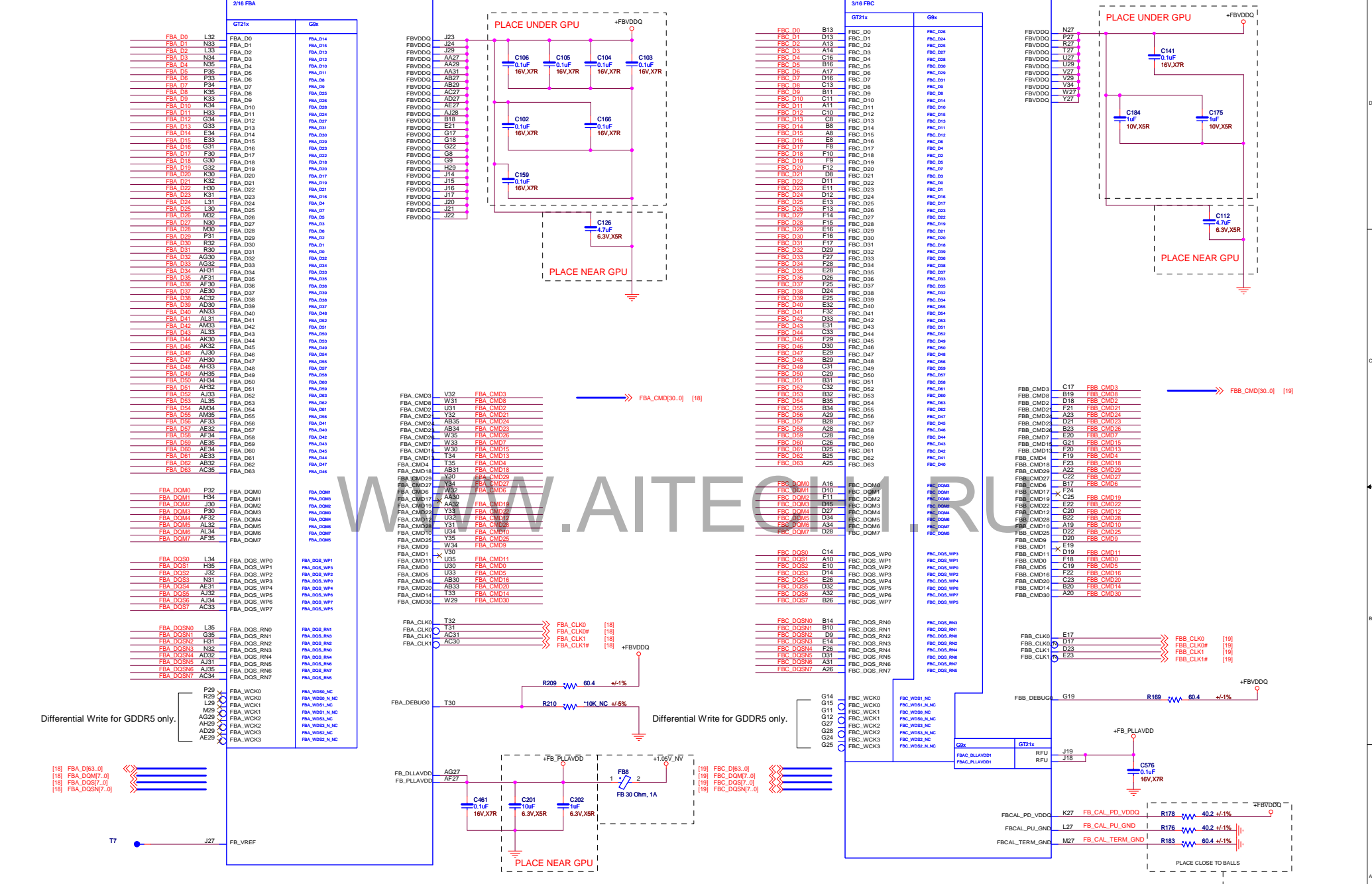



Table 3. Frame Buffer Calibration Resistor Values

Memory Type	FBVDDQ	FBAL_PU_GND	FBAL_PD_VDDQ	FBAL_TERM_GND
DDR3	1.5 V	40.2 Ω	40.2 Ω	60.4 Ω



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17 – N11P 210(DDR3)

Size    Document Number    Rev 1A


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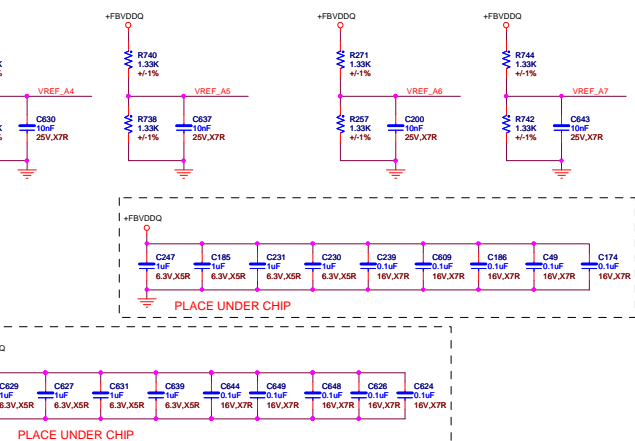
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### Memory Partition-A Upper Data Bits



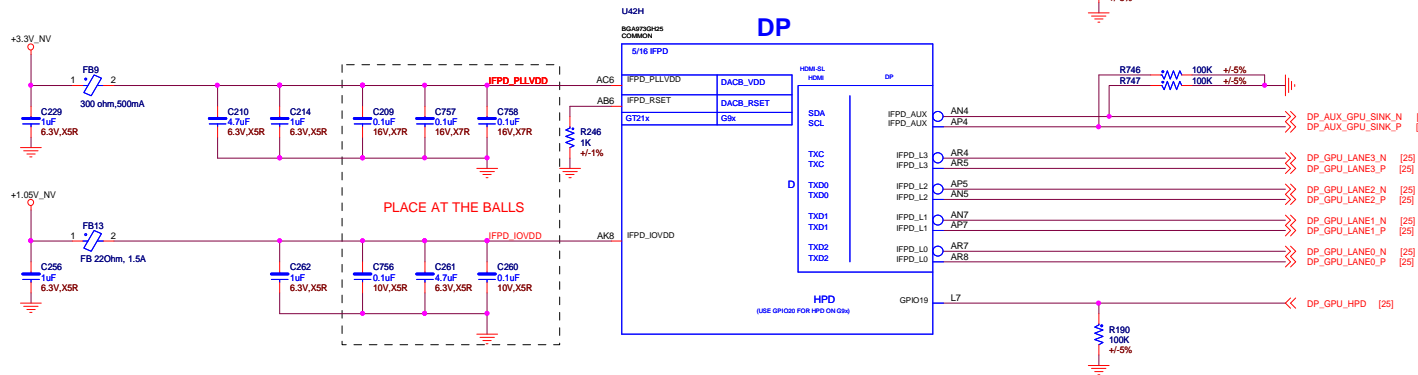
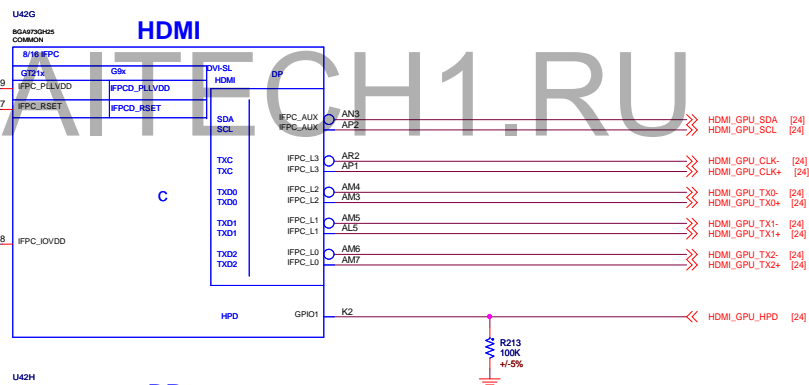
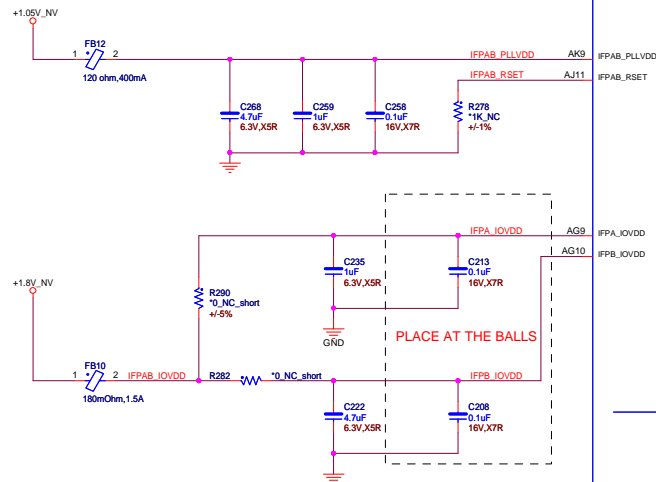
Table 5.4 Mode E Command Mapping

				Ever Light Technology Limited	
Title					
18 -- N11P 3/10(VRAM-A)					
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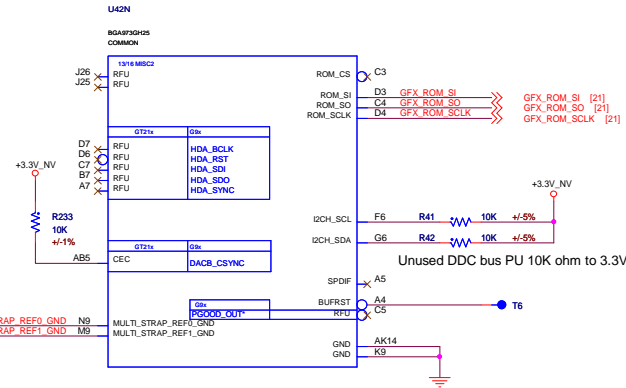
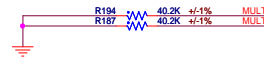




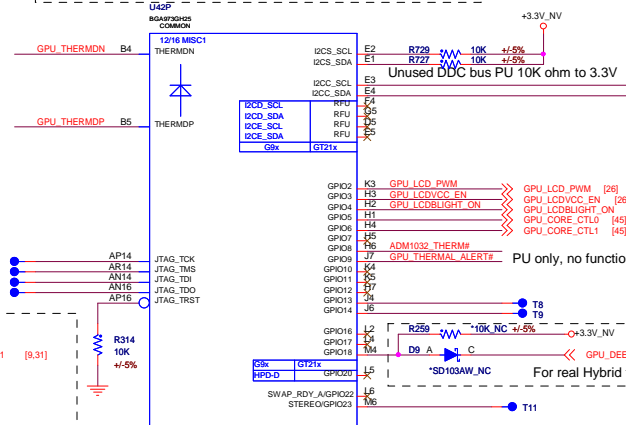
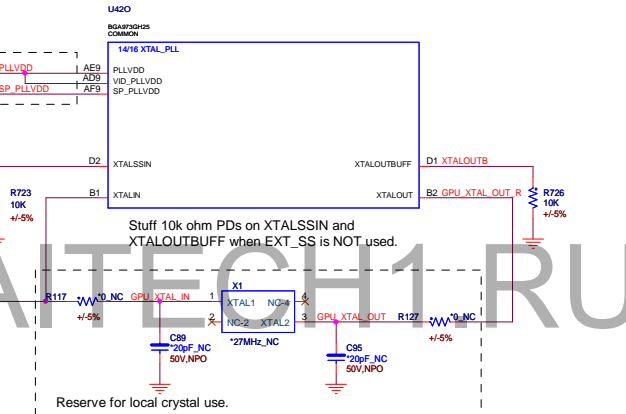
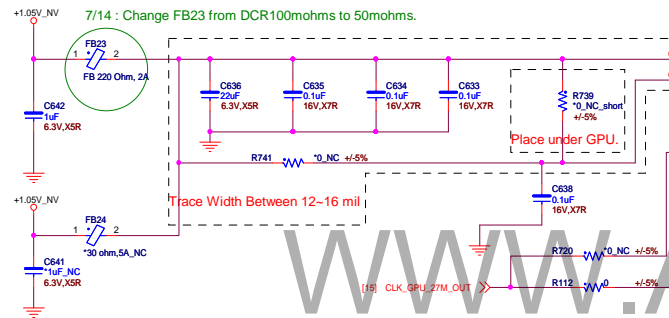




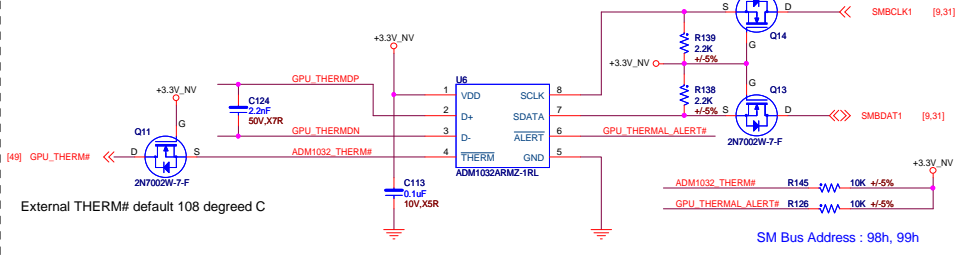
Mode	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND	Strapping Resistor for other STRAP pins
Binary Production Strapping	40.2 kΩ 1% to GND	NC	10 kΩ 5%
Multi-level Strapping	40.2 kΩ 1% to GND	40.2 kΩ 1% to GND	Refer to section13.1



7/14 : Change FB23 from DCR100mohms to 50mohms.



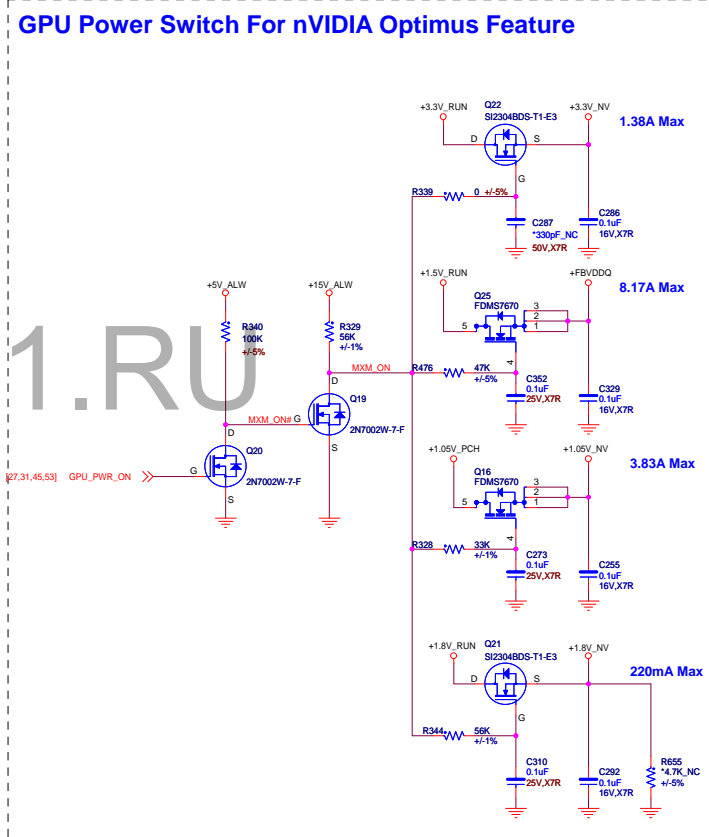
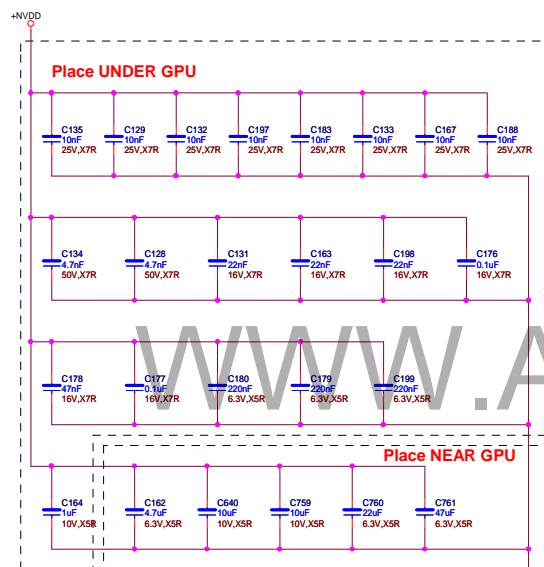
## GPU Thermal Sensor



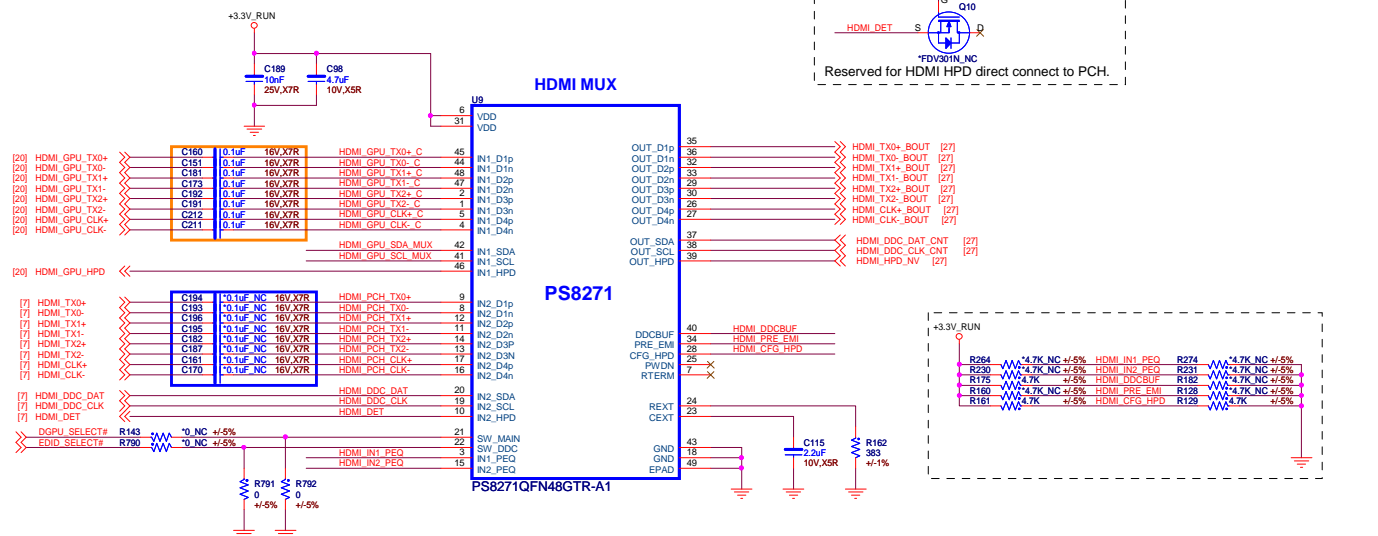
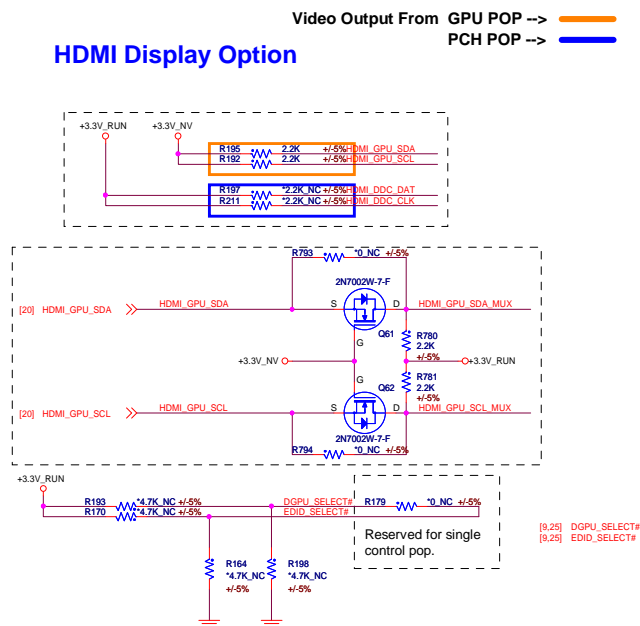
22 -- N11P 7/10(MISC/PLL)

Size Document Number Rev 1A

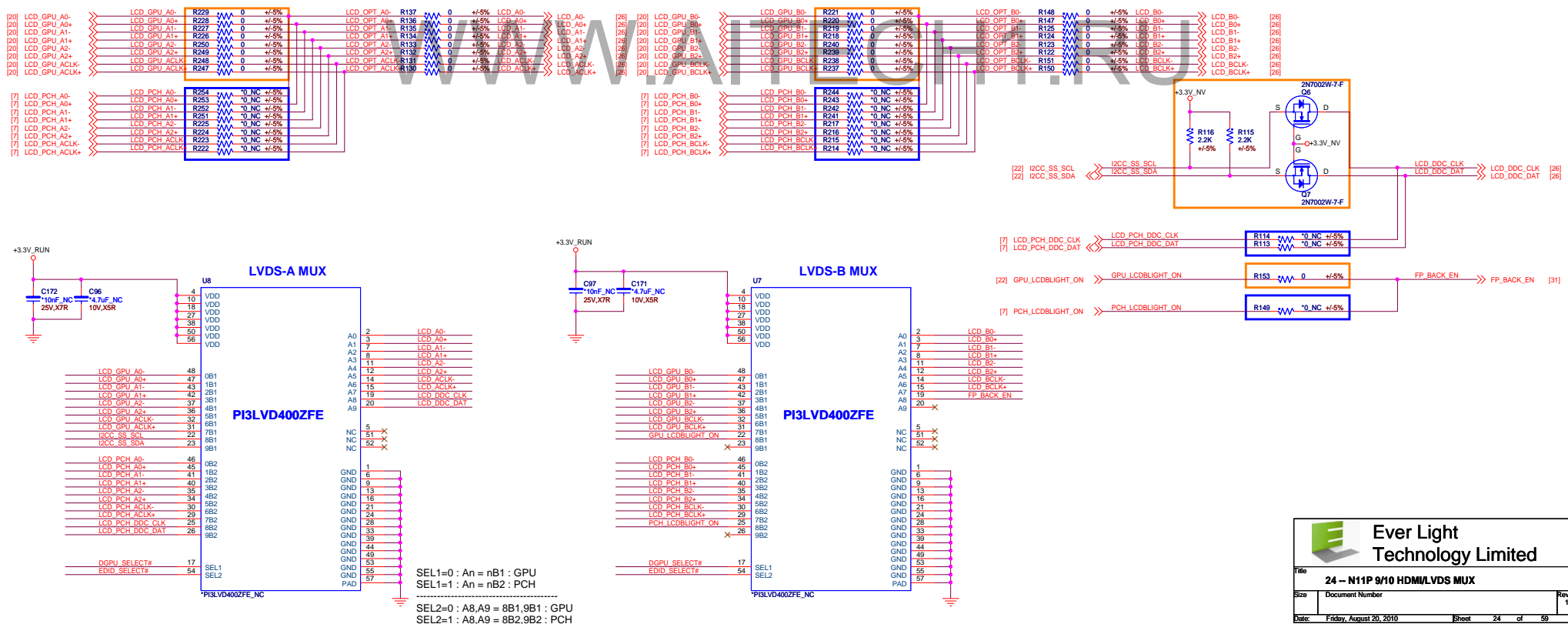
Date: Friday, August 20, 2010 Sheet 22 of 59



## HDMI Display Option

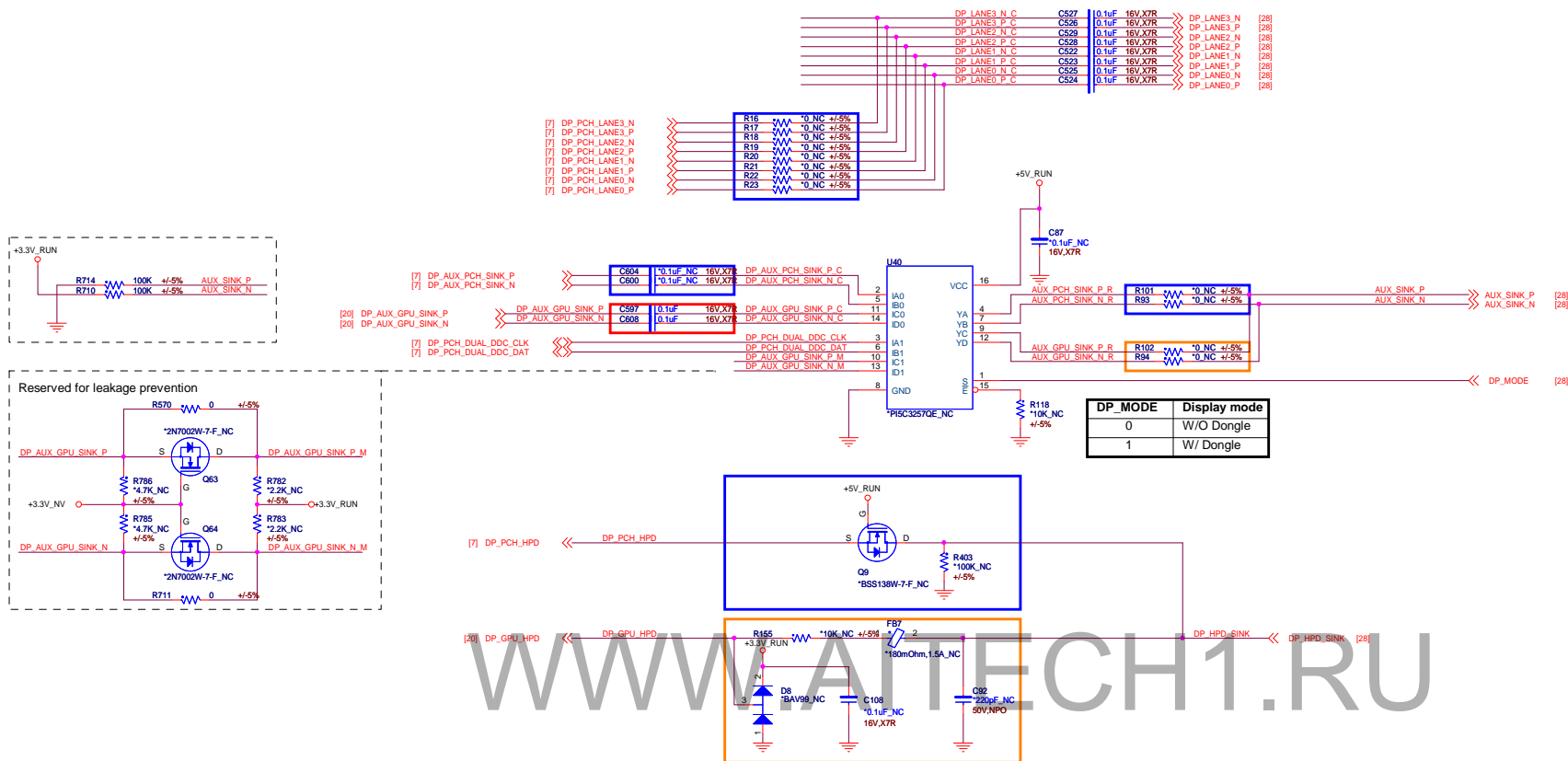


## LVDS Display Option

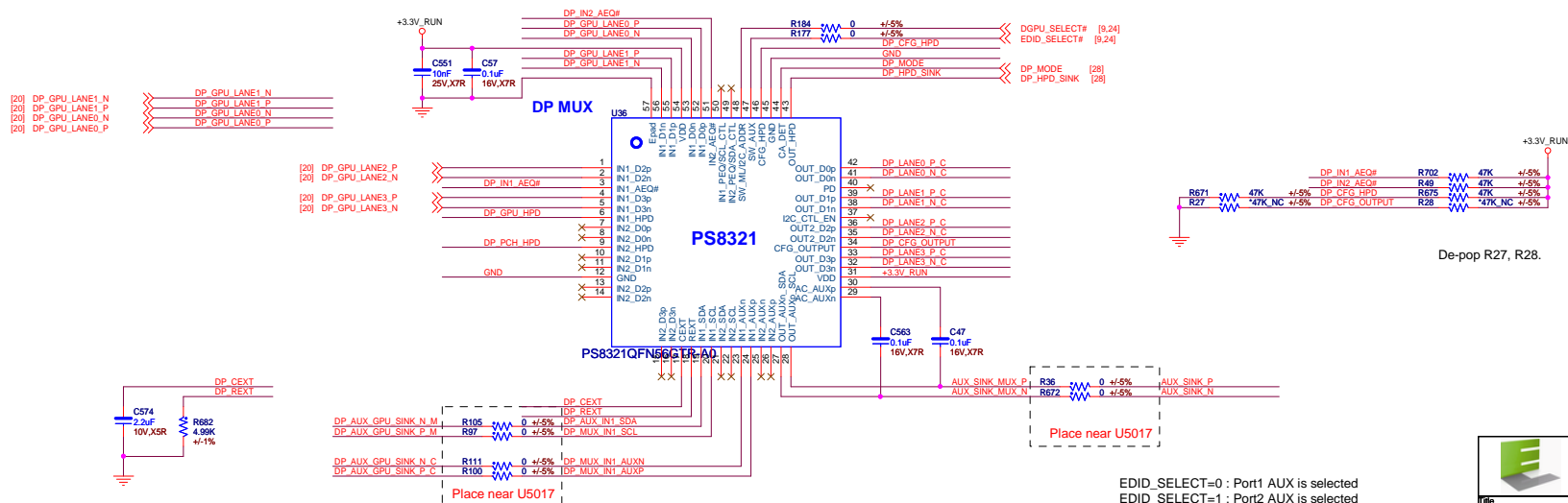





Video Output From GPU POP --> — **DIS or UMA only**  
PCH POP --> —



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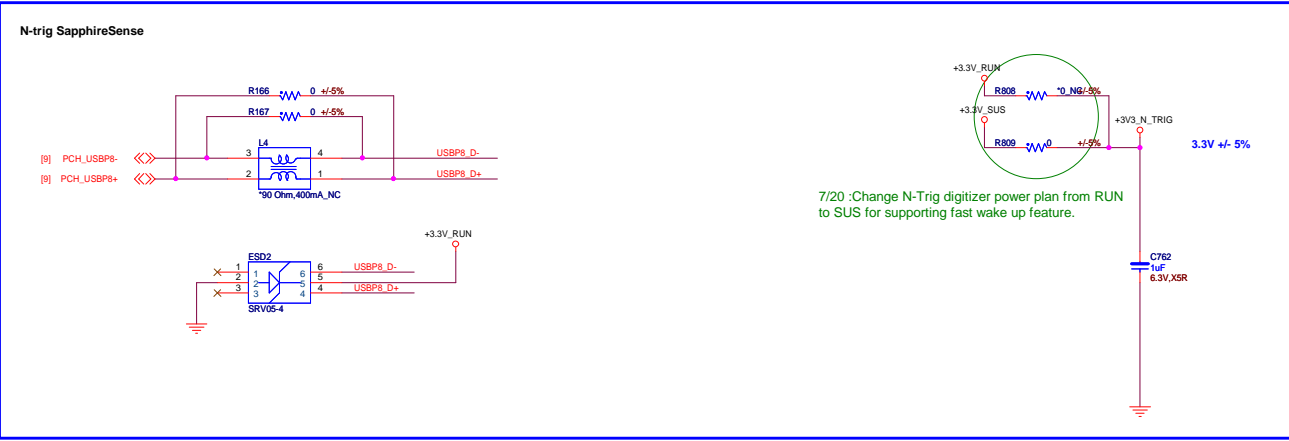
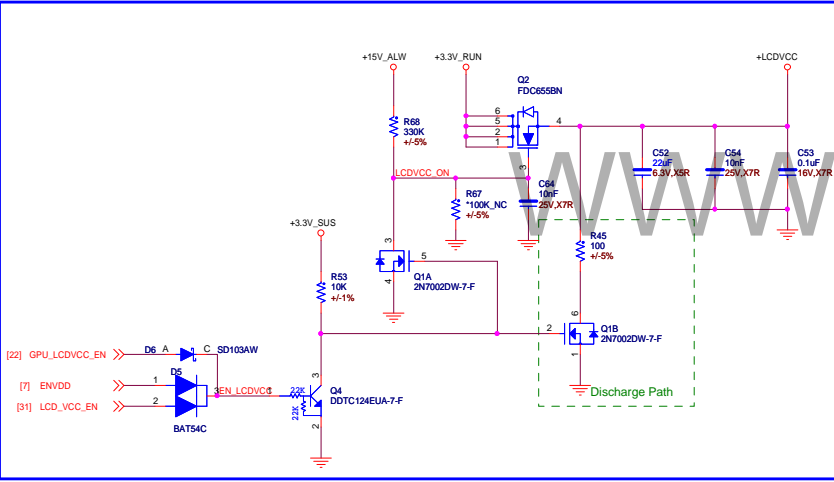
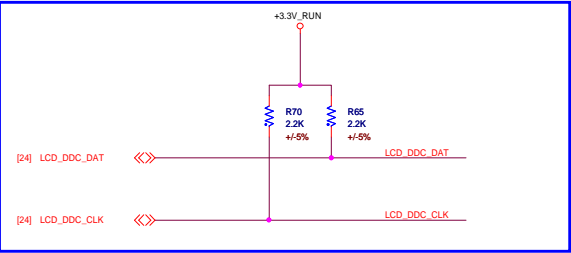
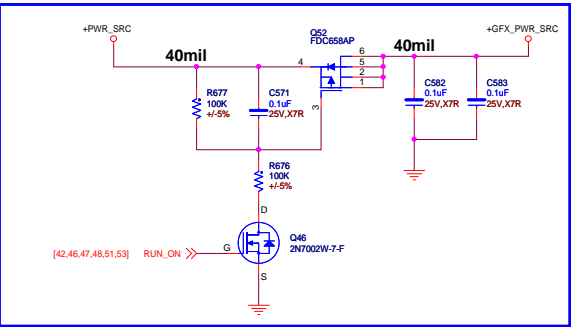
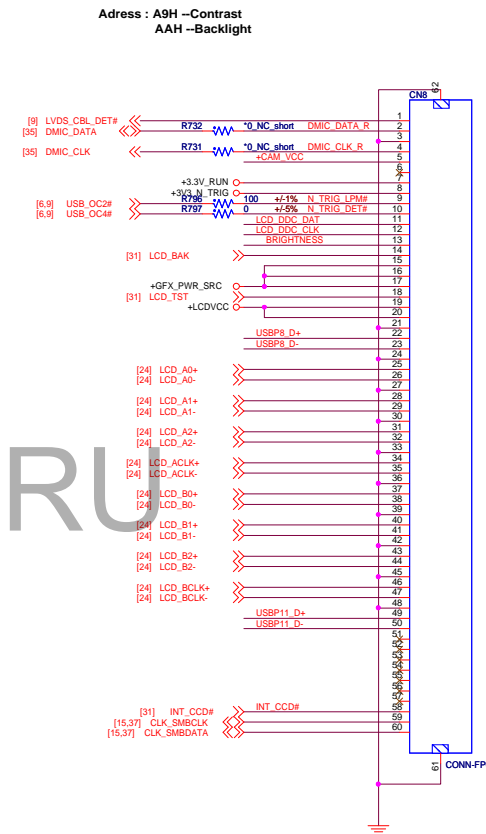
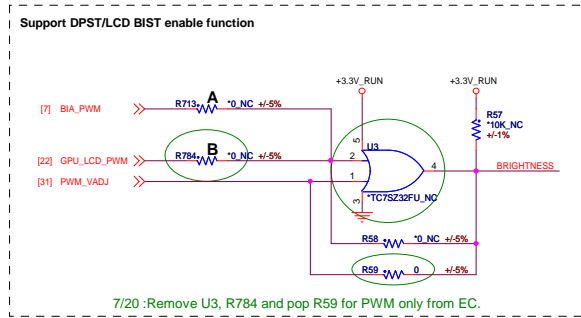
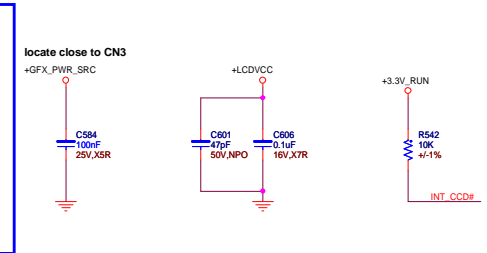
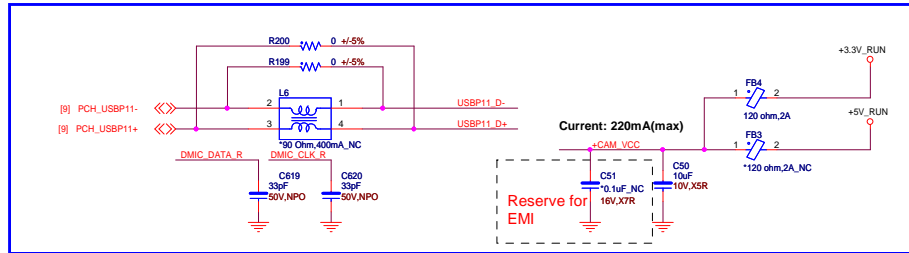


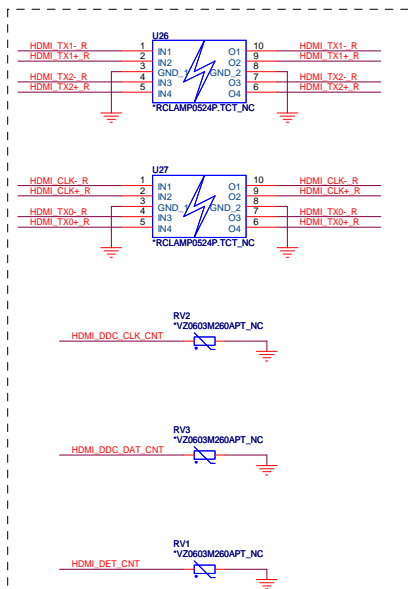
EDID\_SELECT=0 : Port1 AUX is selected  
EDID\_SELECT=1 : Port2 AUX is selected  
dGPU\_SELECT#=0 : Port1 main lane and HPD is selected.  
dGPU\_SELECT#=1 : Port2 main lane and HPD is selected.



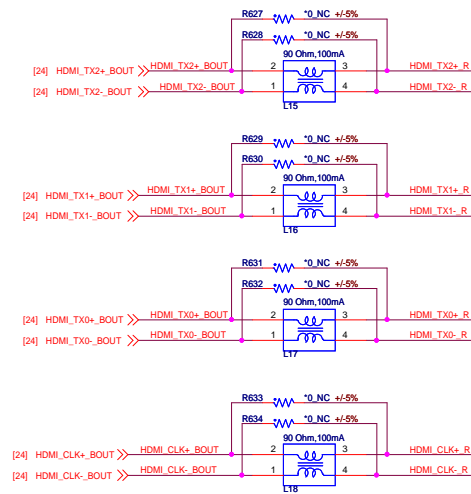
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File		25 -- N11P 10/10 (DP MUX)	
Size	Document Number	Rev 1A	
Date	Friday, August 20, 2010	Sheet	25 of 59

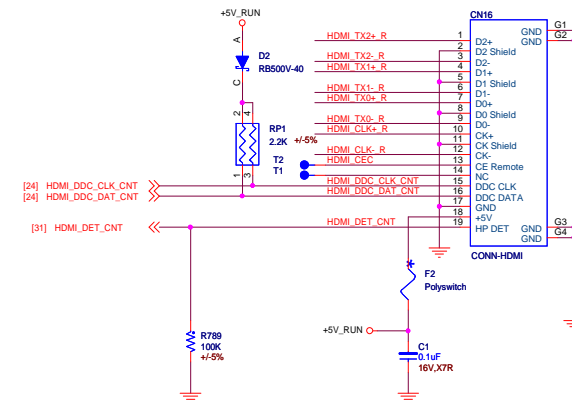




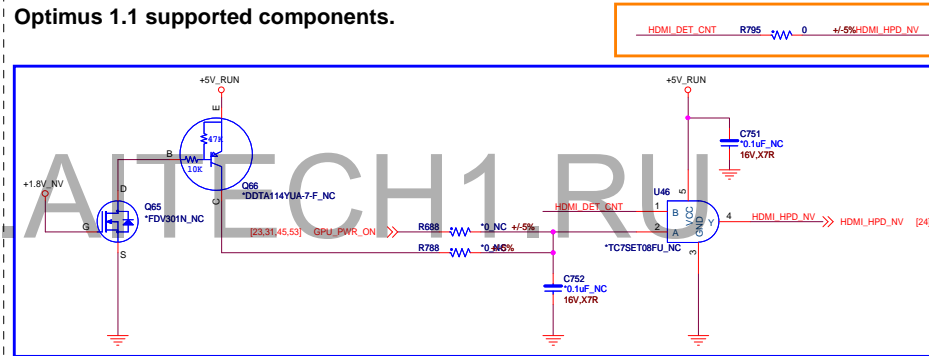
Reserve for EMI and close to HDMI CONN



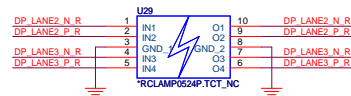
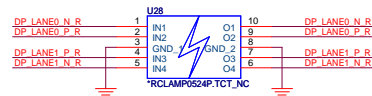
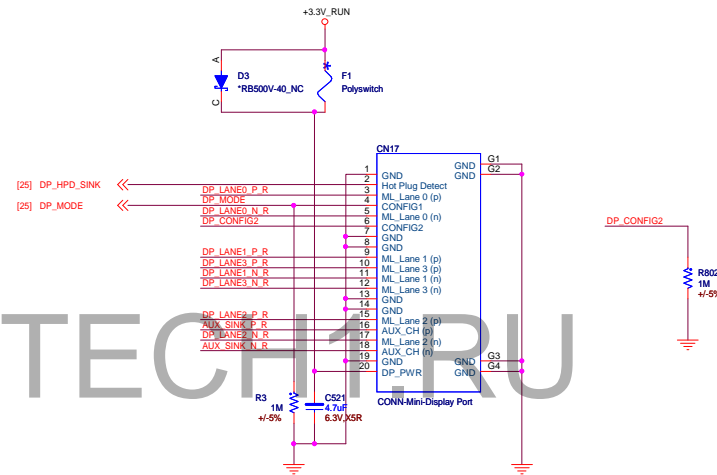
# HDMI



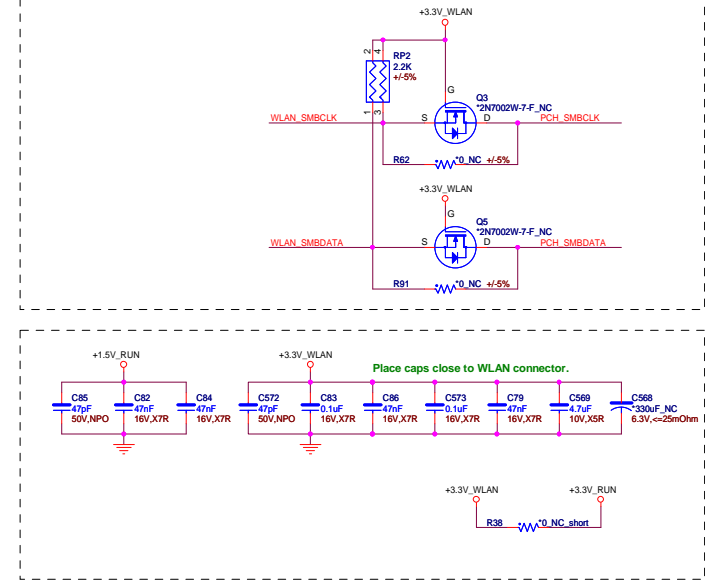
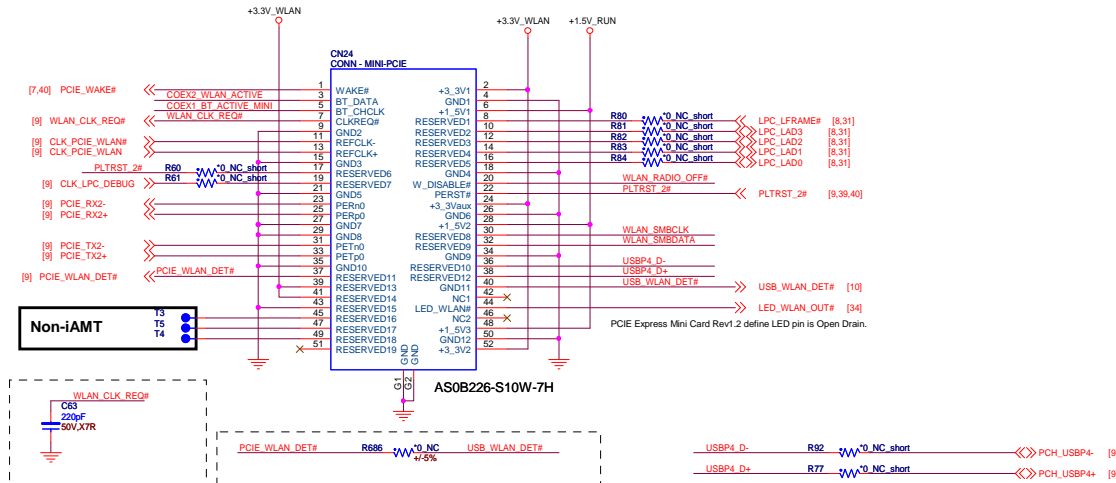
## Optimus 1.1 supported components.



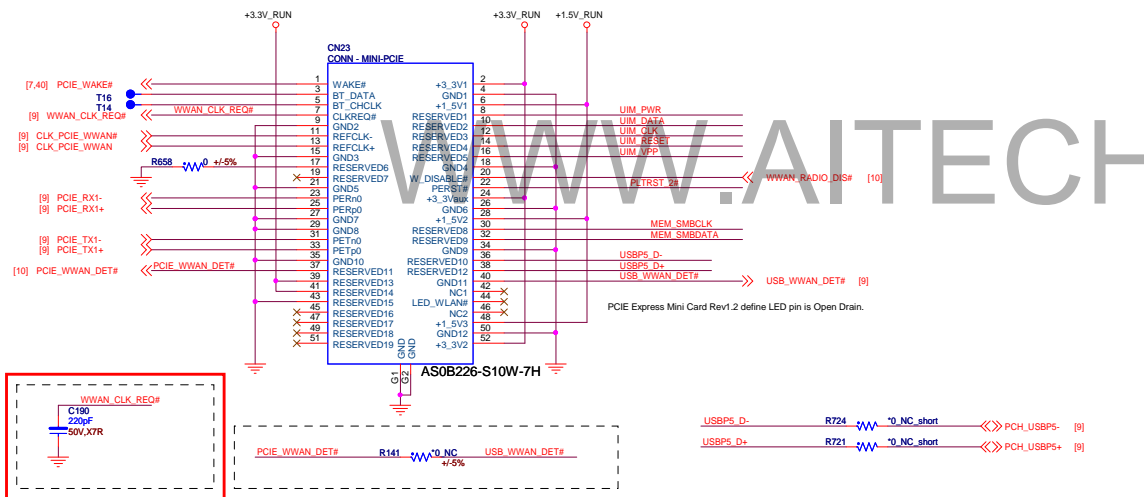
# Mini DP



## MiniCard WLAN connector

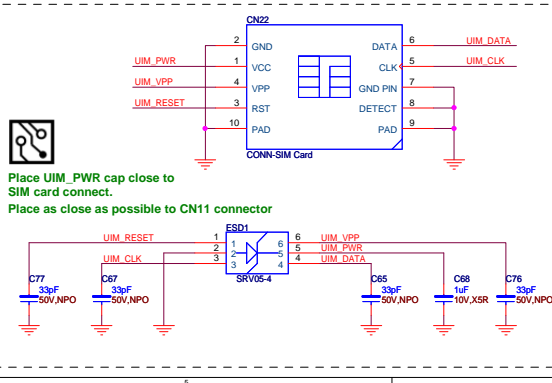
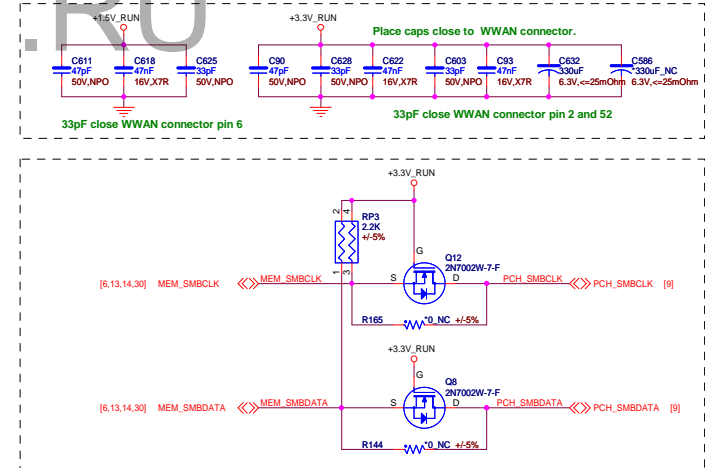


## MiniCard WWAN connector



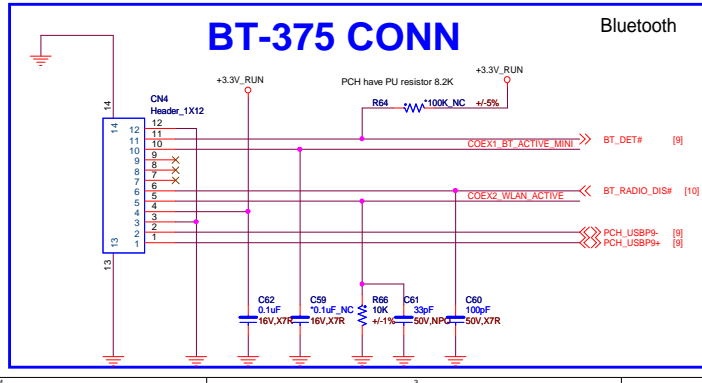
## Support for WoW

Prevent backdrive when  
WoW is enabled.



## BT-375 CONN

Bluetooth



Pin Name	MB Side	Pin No.	Module Side	Pin No.
GND	12	1		
MOD_DET	11	2		
COEX1_BT_ACTIVE	10	3		
BT_COEX_STATUS2	9	4		
BT_PRI_STATUS	8	5		
LINK_IND	7	6		
RADIO_DIS	6	7		
COEX2_WLAN_ACT	5	8		
VMAIN	4	9		
GND	3	10		
HUSB_DN	2	11		
HUSB_DP	1	12		

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29 -- WLAN, WWAN, SIM, BT

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Rev 1A

[illegible]

I2C Address Setting	
SDO = H	SDO = L
Addr = 0011101	Addr = 0011100

U19	Pin	Signal
INT1	8	VDD
INT2	9	RSDV(VDD)
CS	10	VDD_IO
SDO	12	GND_0
SDI/SDA/SDO	13	GND_1
SPC/SCL	14	GND_2
DESSYDLTR	15	GND_3

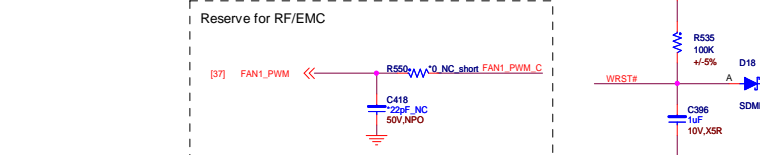
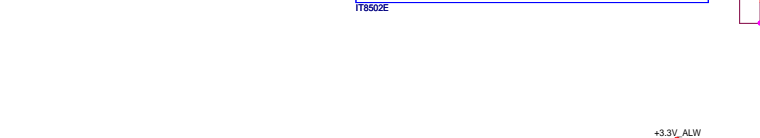
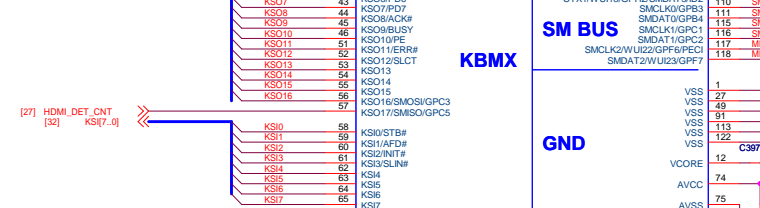
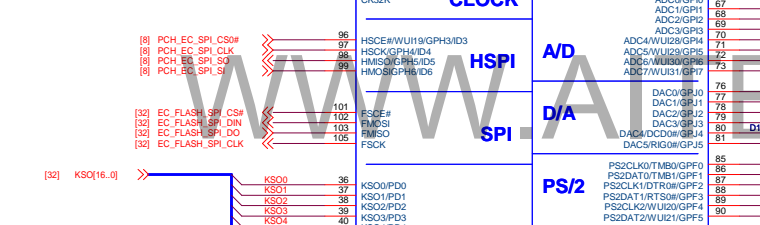
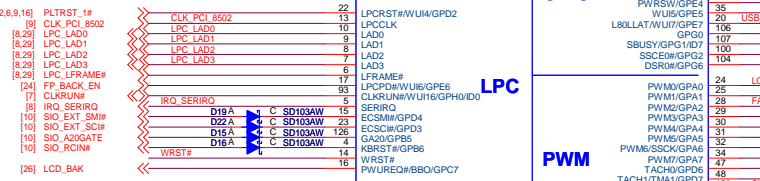
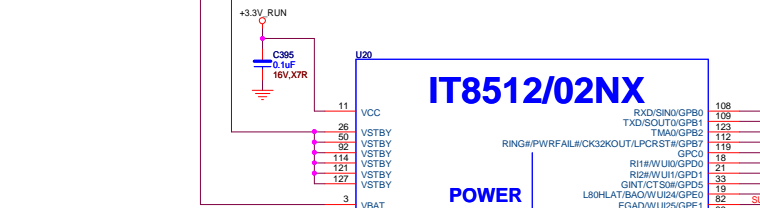
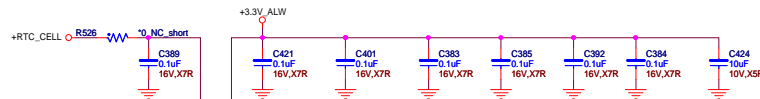
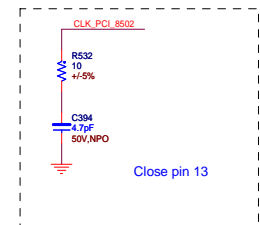
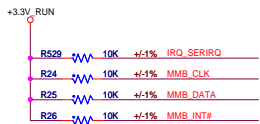
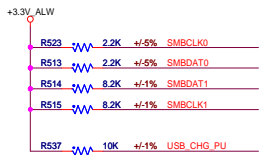
Additional connections and components shown in the diagram:

- [9] PCH\_IRQ\_E\_GPIO2 connected to R512 (10K) and \*0\_NC\_short.
- [10] HDD\_FFS\_INT connected to HDD\_FFS\_INT.
- +3.3V\_RUN connected to R524 (10K) and \*+1%.
- R490 (10K) connected to \*10K\_NC and \*+1%.
- [6.13.14.29] MEM\_SMBDATA connected to SDO.
- [6.13.14.29] MEM\_SMBCLK connected to SPC/SCL.
- Capacitors: C365 (10uF, 16V X7R) and C371 (10uF, 10V X5R).

[illegible]

Title			
30 -- HDD, ODD (SATA)			
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# IT8512/02NX

## POWER

## GPIO

## LPC

## PWM

## CLOCK

## A/D

## D/A

## HSPI

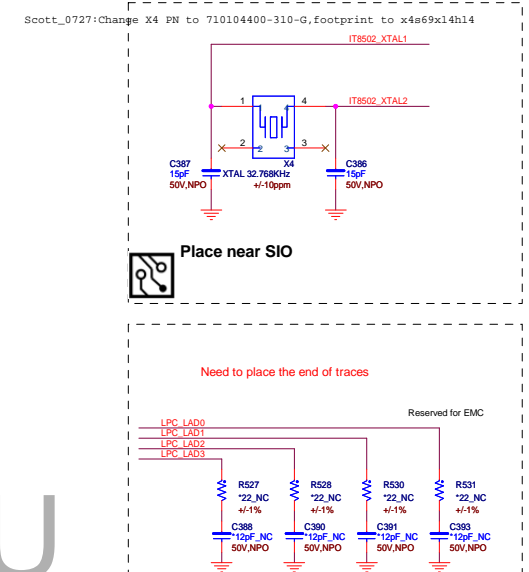
## SPI

## PS/2

## SM BUS

## KBMX

## GND



**Board ID Straps**

PCBA = A\_RES from 1K to 10K  
PCB = B\_RES from 1K to 10K

A_RES	PCBA	B_RES	PCB
100K	MBC (CLK) 2G VRAM	100K	X-build(A00)
33K	TBD	33K	ST2
20K	TBD	20K	ST
12K	TBD	12K	TBD
8.2K	TBD	8.2K	PT
5.1K	TBD	5.1K	TBD
2.7K	TBD	2.7K	SS12 (X01)
1K	MBA (UMA)	1K	SS11 (X00)
0	TBD	0	TBD

7/14 : R551 from 5% to 1%.

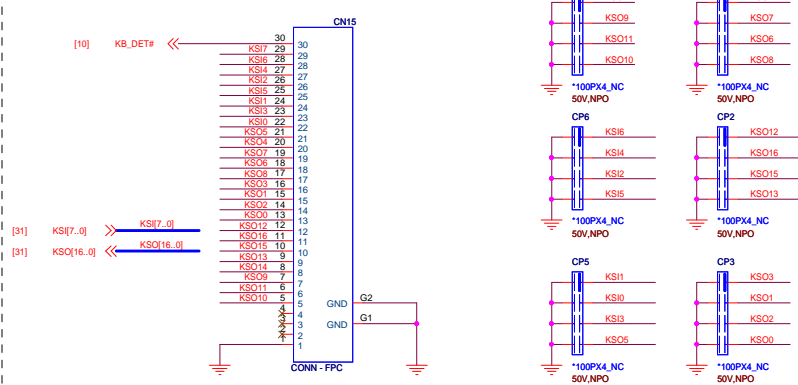
**Ever Light Technology Limited**

File: 31 -- SIO (IT8502)

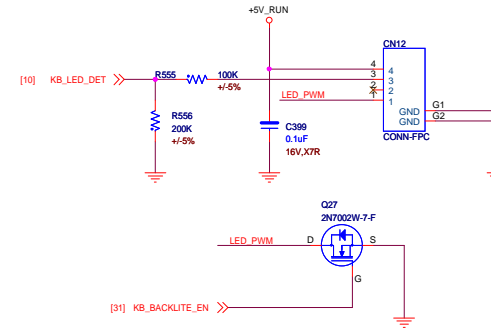
Size: Document Number: Rev 1A

Date: Friday, August 20, 2010 Sheet: 31 of 59

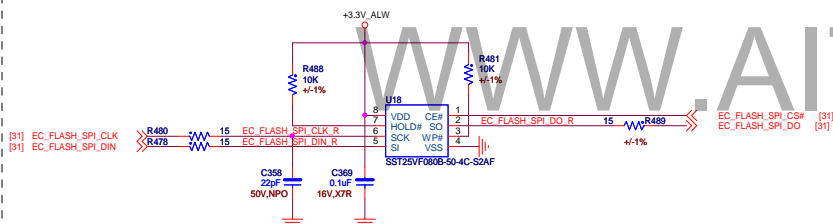
## Keyboard connect



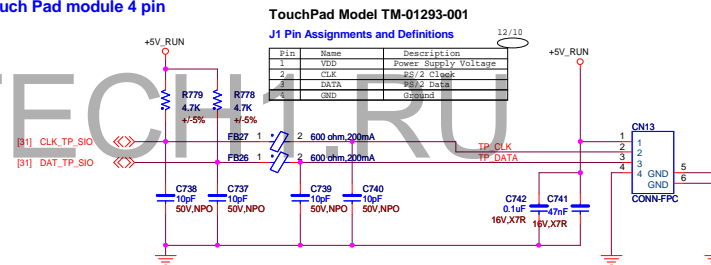
## BACKLITE CONNECT



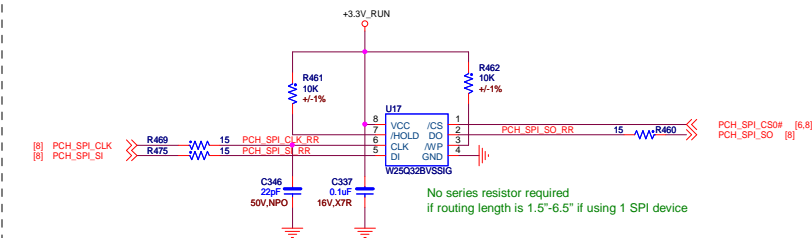
## EC SPI ROM, (1M Byte)



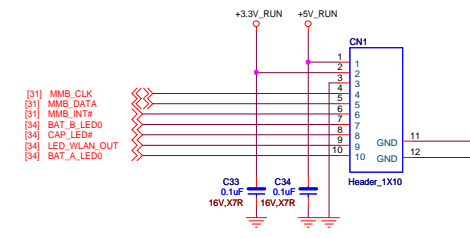
## Touch Pad module 4 pin



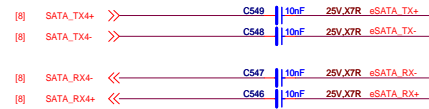
## PCH SPI ROM, (4M Byte)



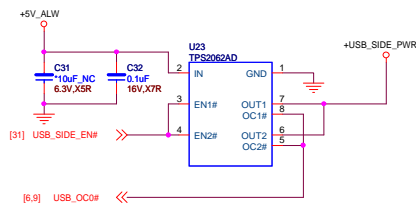
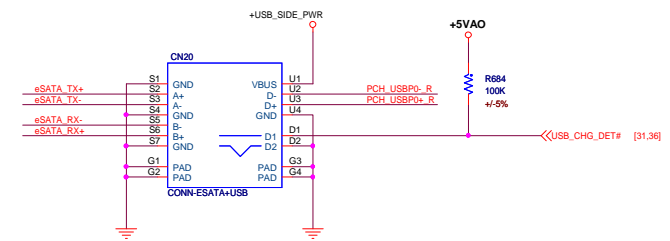
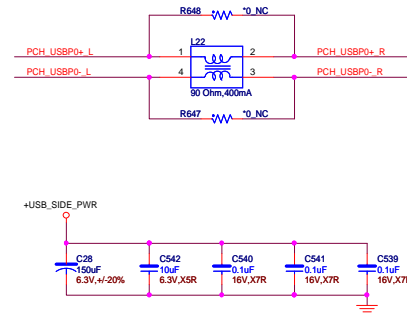
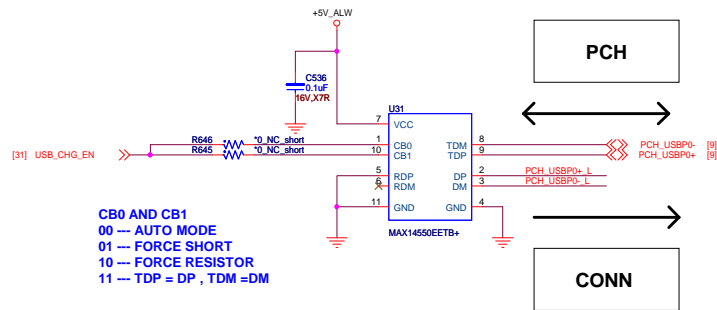
## MMB module 10 pin



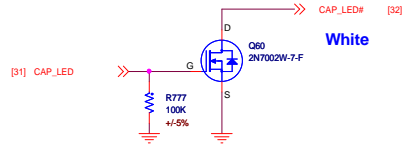
# SATA Re-Driver(Removed Per EA has passed w/o re-driver)



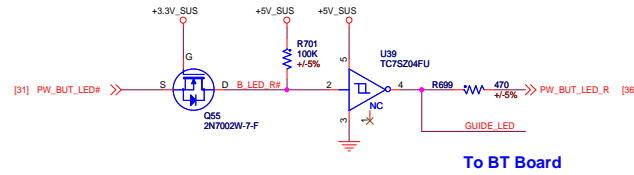
WWW.AITECH1.RU eSATA + USB Charge Conn



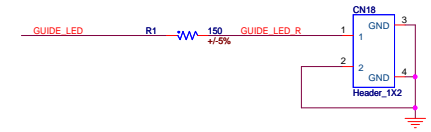
## MMB \ CAP



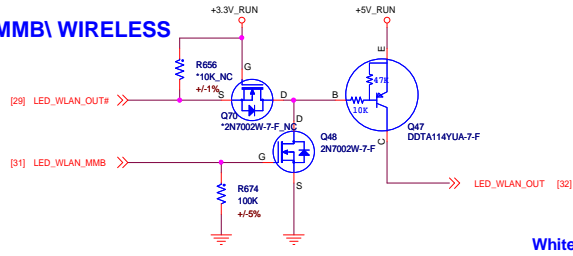
## POWER \ BUTTON



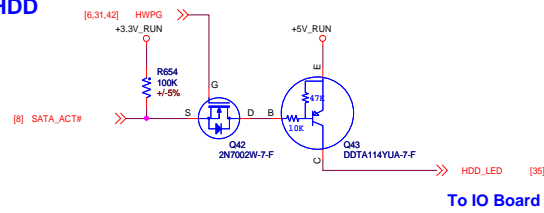
## LIGHT GUIDE LED



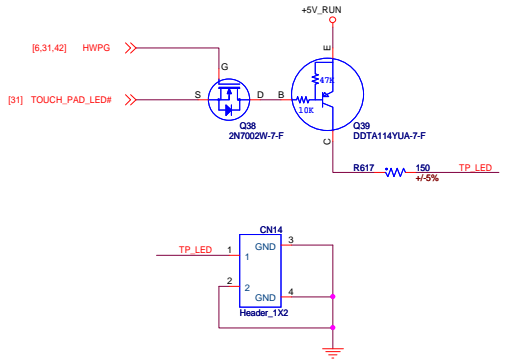
## MMB \ WIRELESS



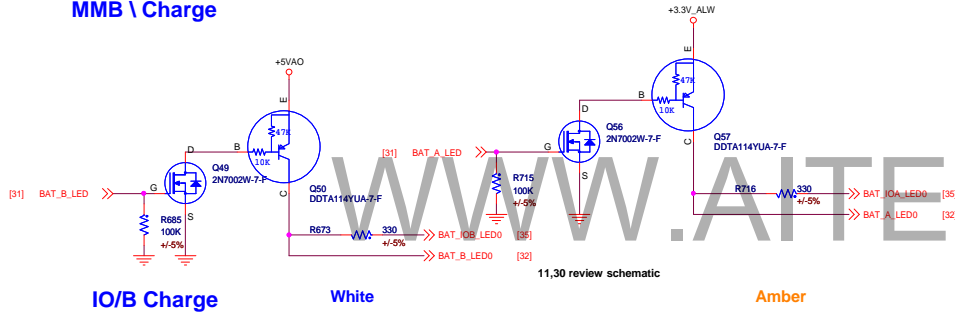
## HDD



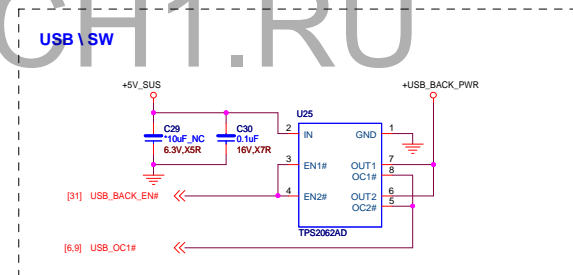
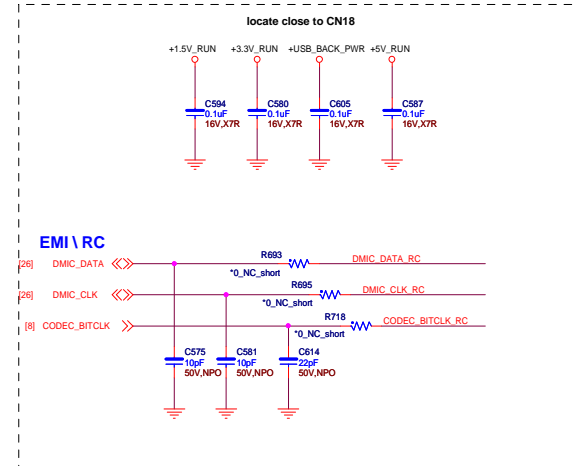
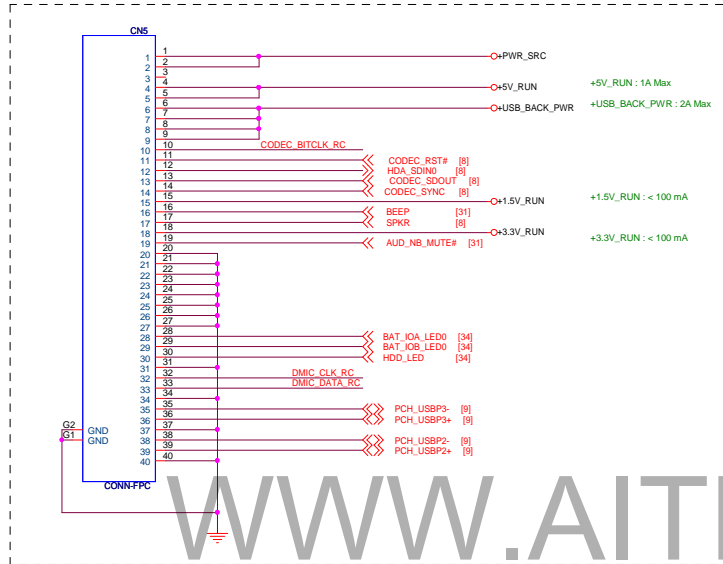
## Touch Pad LED



## MMB \ Charge

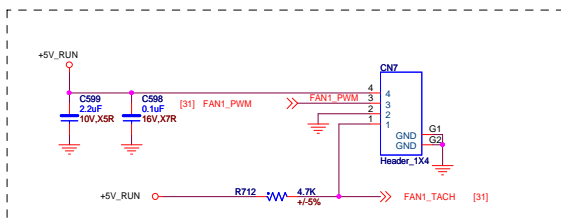


# IO Board Conn

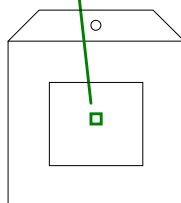




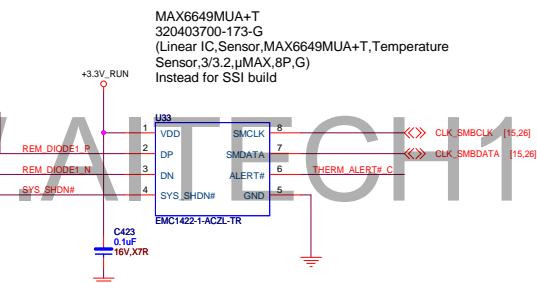




Place center on CPU Socket  
at the same layer (OTP)



CAP close to  
EMC1422 PIN#2.

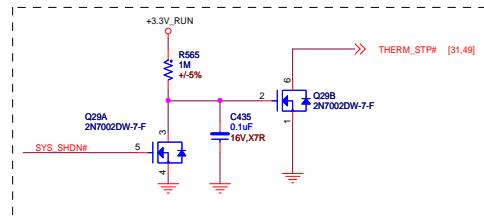


OTP 90 degree C



OTP degree table

SYS_SHDN#	10k ohm
THERM_ALERT#_C	
6.8k ohm	90 degree



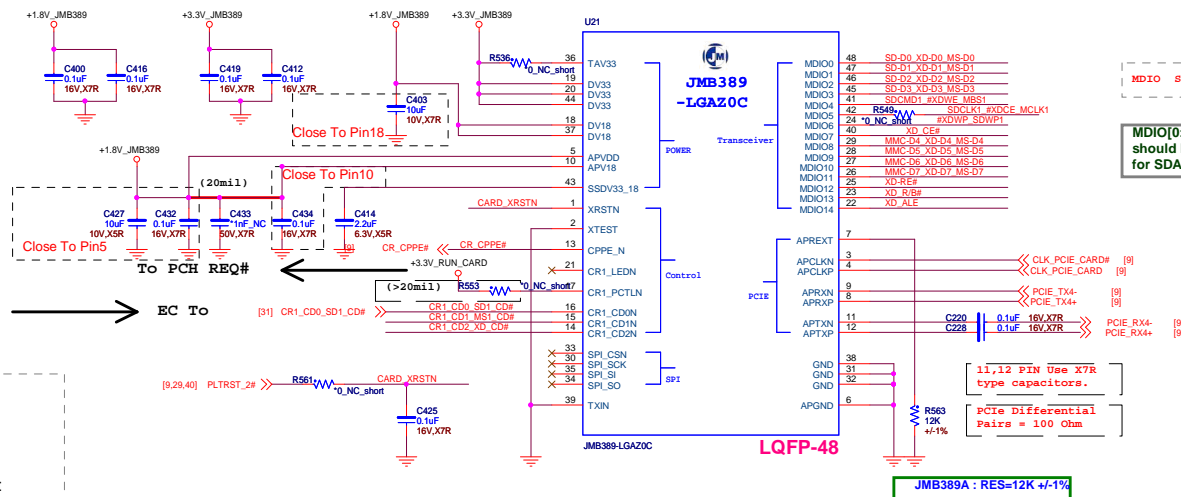
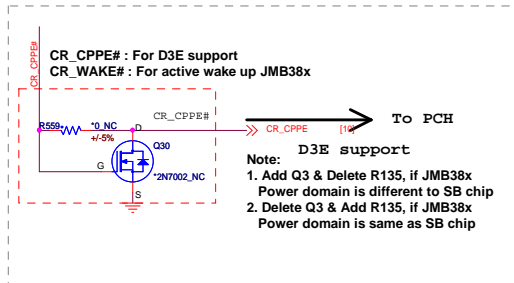
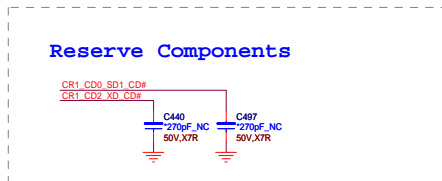
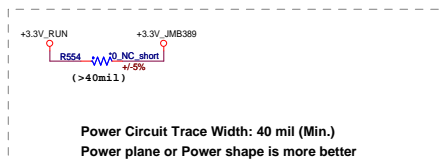
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**37 -- FAN, THERMAL**

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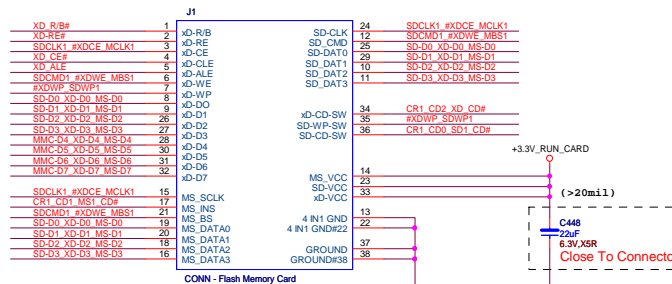
**Blank Page**  
**WWW.AITECH1.RU**



WWW.AITECH1.RU

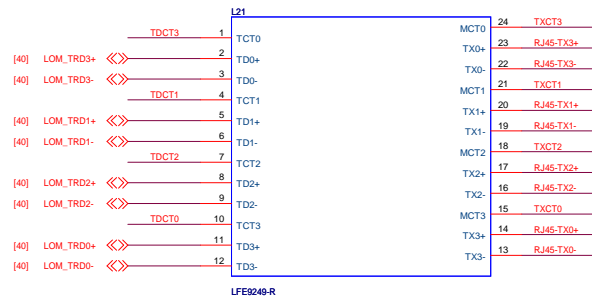
Card Reader Pin Configuration

Pin Name	Default Mode	SD/MMC Card	MSCard	XCARD
MDIO0	SD/MMC/MSxD	SD1_DAT0	MS1_DAT0	XD1_DAT0
MDIO1		SD1_DAT1	MS1_DAT1	XD1_DAT1
MDIO2		SD1_DAT2	MS1_DAT2	XD1_DAT2
MDIO3		SD1_DAT3	MS1_DAT3	XD1_DAT3
MDIO4		SD1_CMD	MS1_BS	XD1_WE#
MDIO5		SD1_CLK	MS1_CLK	XD1_CE#
MDIO6		SD1_WP		XD1_WP#
MDIO7				XD1_CLE
MDIO8		MMC_DAT4	MS1_DAT4	XD_DAT4
MDIO9		MMC_DAT5	MS1_DAT5	XD_DAT5
MDIO10		MMC_DAT6	MS1_DAT6	XD_DAT6
MDIO11		MMC_DAT7	MS1_DAT7	XD_DAT7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE
CR1_LEDN		SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN		SD1_PCTL#	MS1_PCTL#	XD_PCTL#
CR1_CD0		SD1_CD#		
CR1_CD1			MS1_CD#	
CR1_CD2				XD_CD#



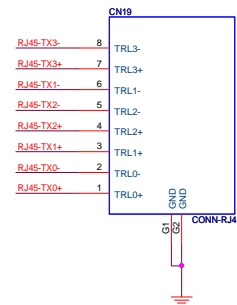


## Transformer

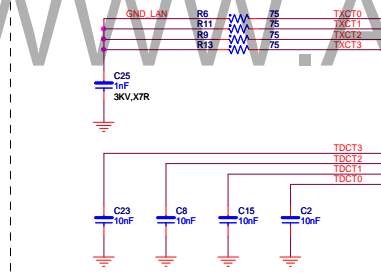


## RJ45

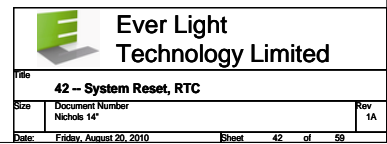
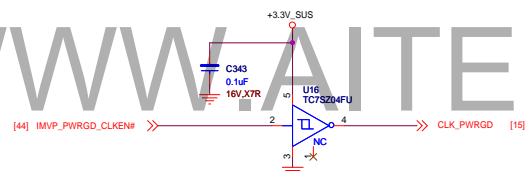
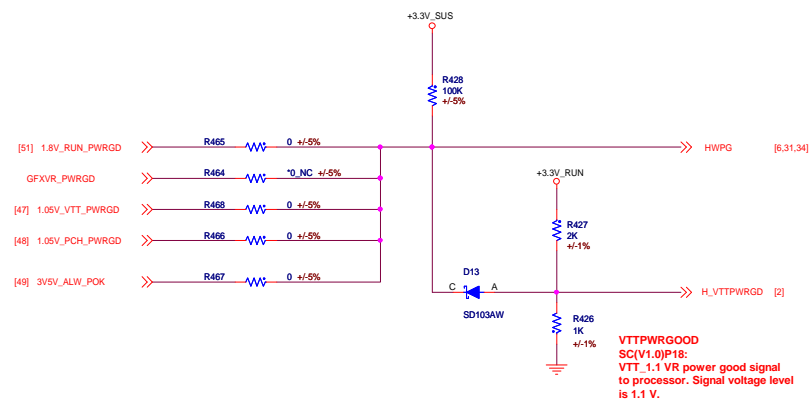
### RJ-45 Connector



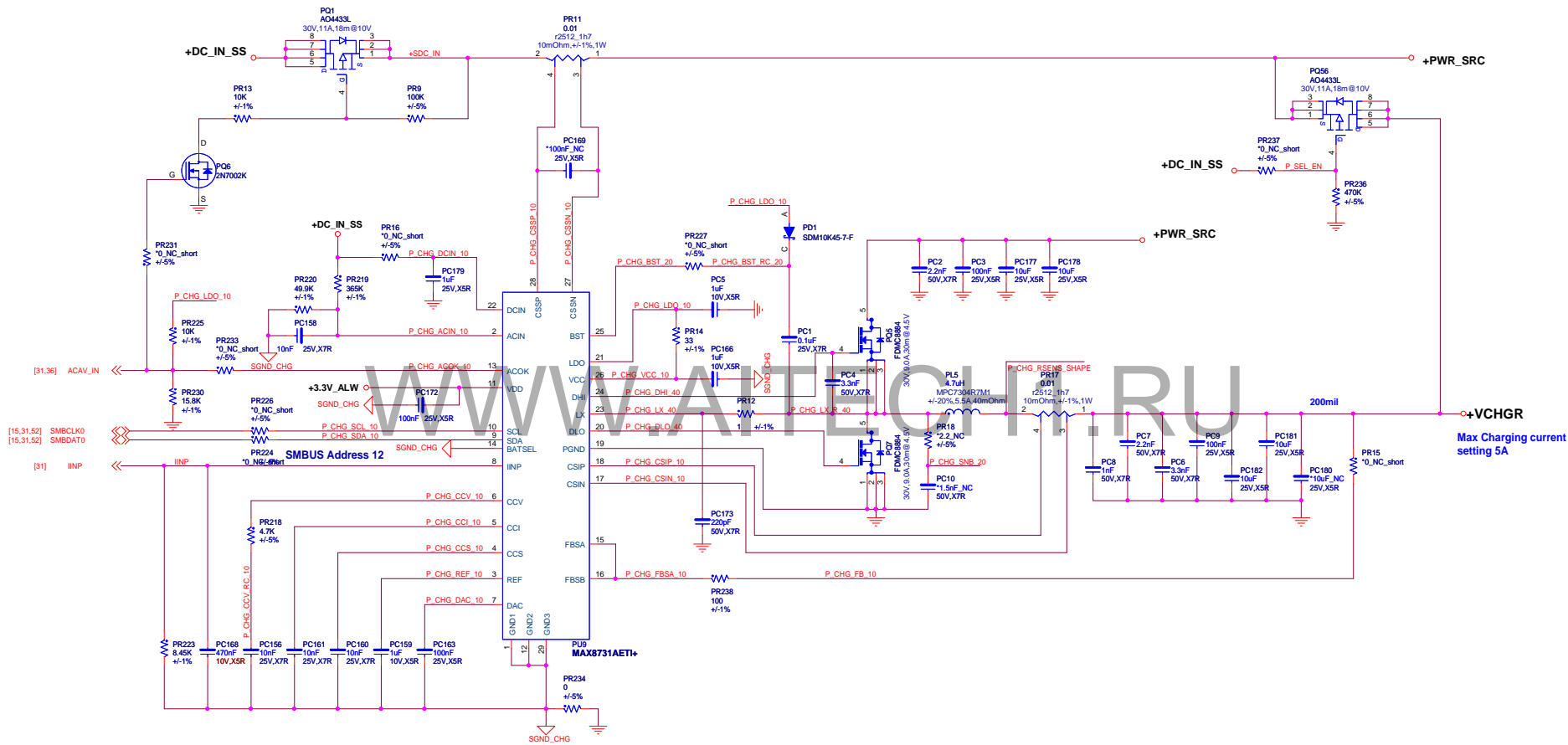
## Reserved EMI



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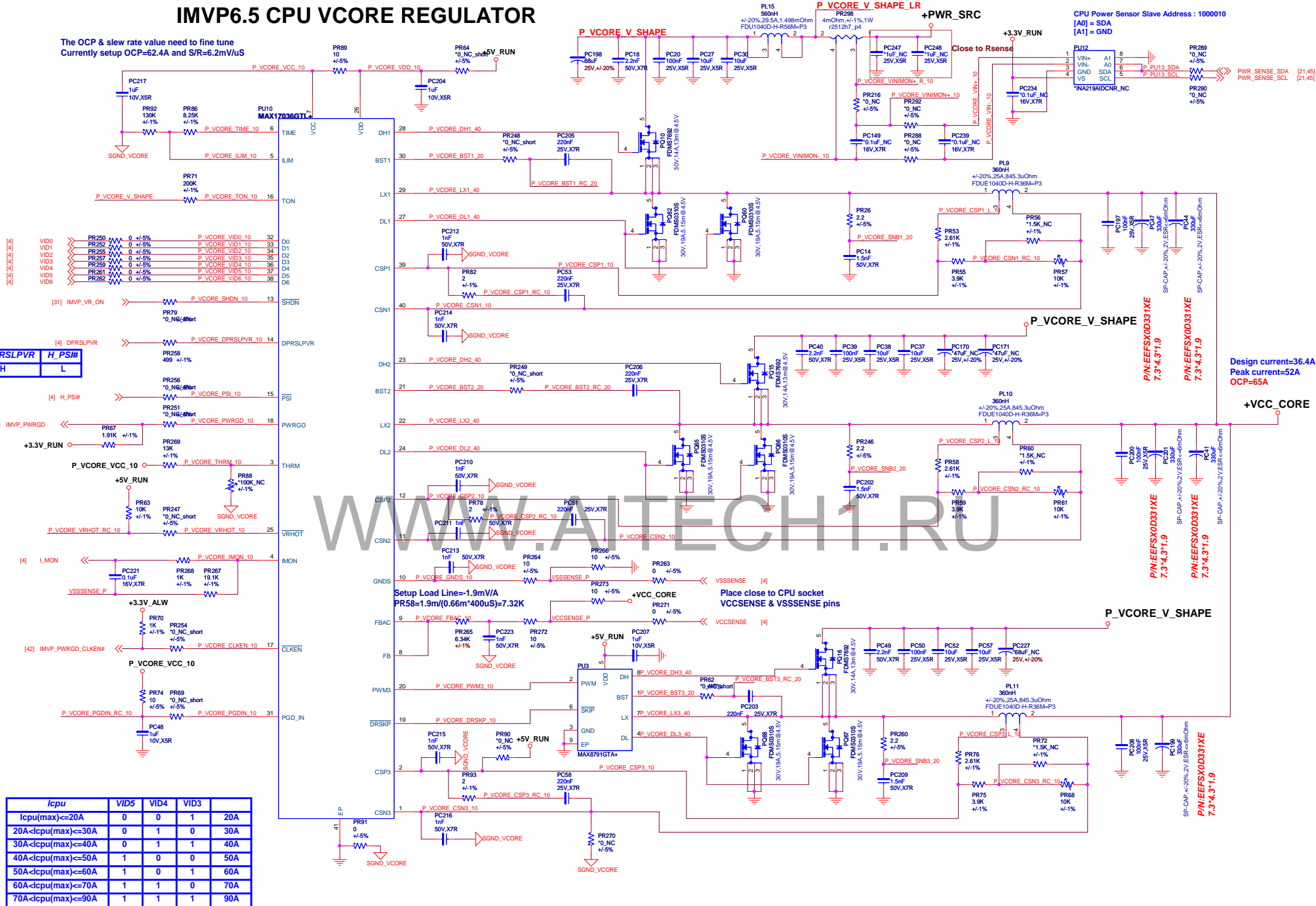




<Variant Name>

# IMVP6.5 CPU VCORE REGULATOR

The OCP & slew rate value need to fine tune  
Currently setup OCP=62.4A and S/R=6.2mV/uS



<Variant Name>

**Ever Light Technology Limited**

44 - PW\_VCORE(MAX17036)

Nichols 14" SW\_ARD\_Eric Ho

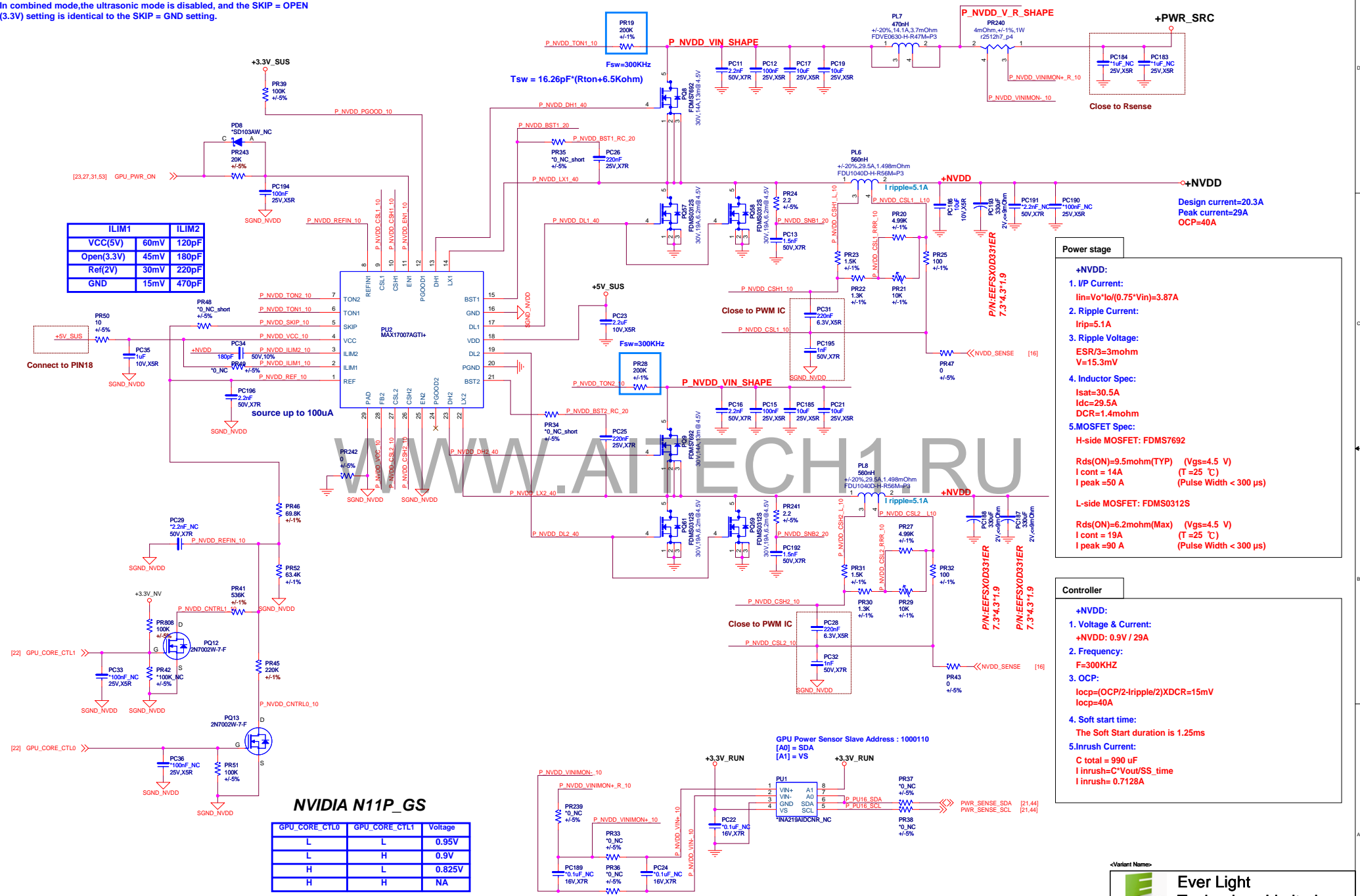
Friday, August 20, 2010

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Rev 1A

VDD (5V) = Forced-PWM operation  
Open (3.3V) = Ultrasonic mode (without forced-PWM during transitions)  
REF (2V) = Pulse-skipping mode (with forced-PWM during transitions)  
GND = Pulse-skipping mode (without forced-PWM during transitions)  
In combined mode, the ultrasonic mode is disabled, and the SKIP = OPEN (3.3V) setting is identical to the SKIP = GND setting.

+NVDD POWER SUPPLY



ILIM1	ILIM2
VCC(5V)	60mV
Open(3.3V)	45mV
Ref(2V)	30mV
GND	15mV

NVIDIA N11P_GS		
GPU_CORE_CTL0	GPU_CORE_CTL1	Voltage
L	L	0.95V
L	H	0.9V
H	L	0.825V
H	H	NA

Power stage

+NVDD:

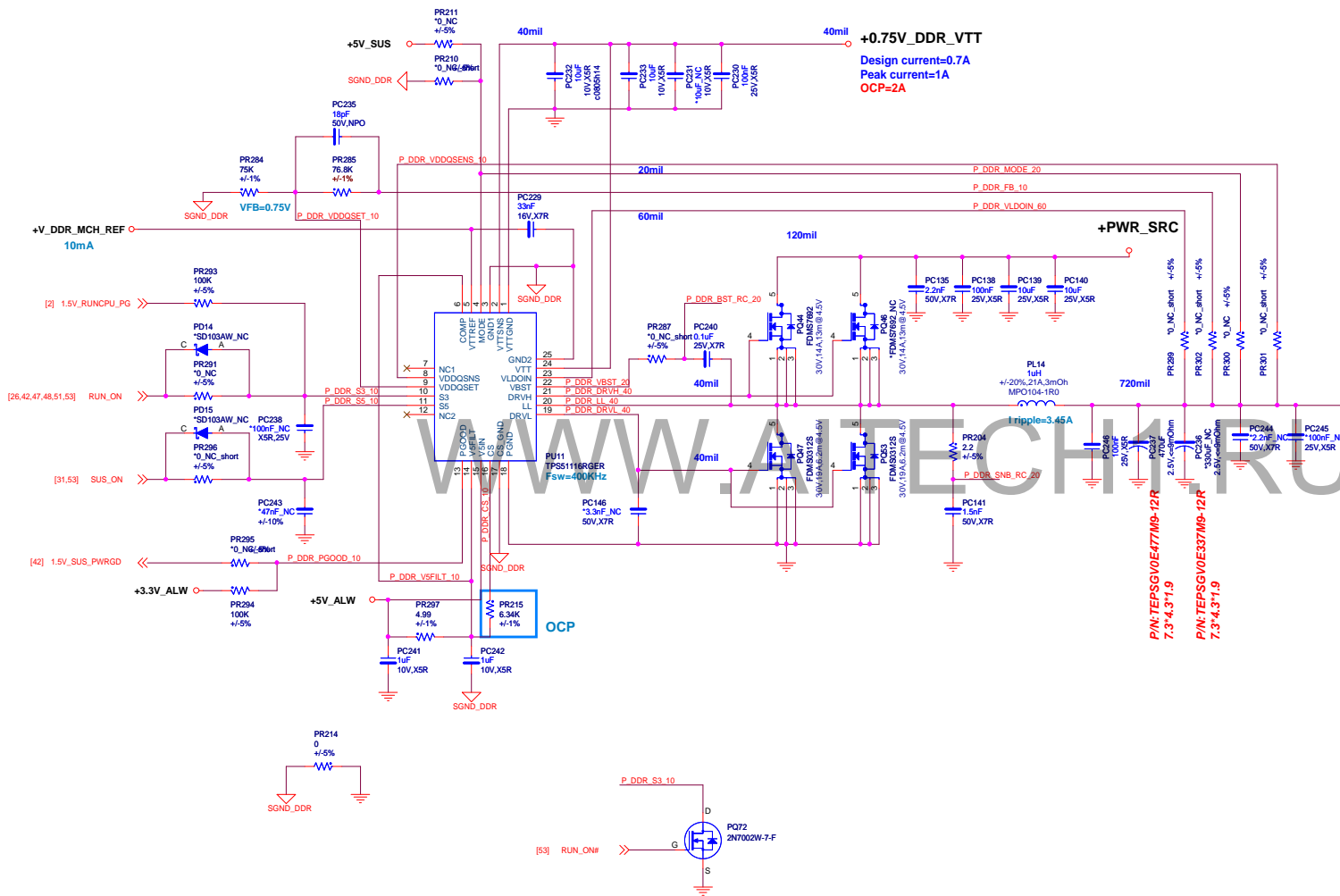
1. IP Current:  
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 3.87A$
2. Ripple Current:  
 $I_{rip} = 5.1A$
3. Ripple Voltage:  
 $ESR/3 = 3mohm$   
 $V = 15.3mV$
4. Inductor Spec:  
 $I_{sat} = 30.5A$   
 $I_{dc} = 29.5A$   
 $DCR = 1.4mohm$
5. MOSFET Spec:  
H-side MOSFET: FDM57692  
 $R_{ds}(ON) = 9.5mohm(TYP)$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 14A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 50A$  (Pulse Width < 300  $\mu s$ )  
L-side MOSFET: FDM50312S  
 $R_{ds}(ON) = 6.2mohm(Max)$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 19A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 90A$  (Pulse Width < 300  $\mu s$ )

Controller

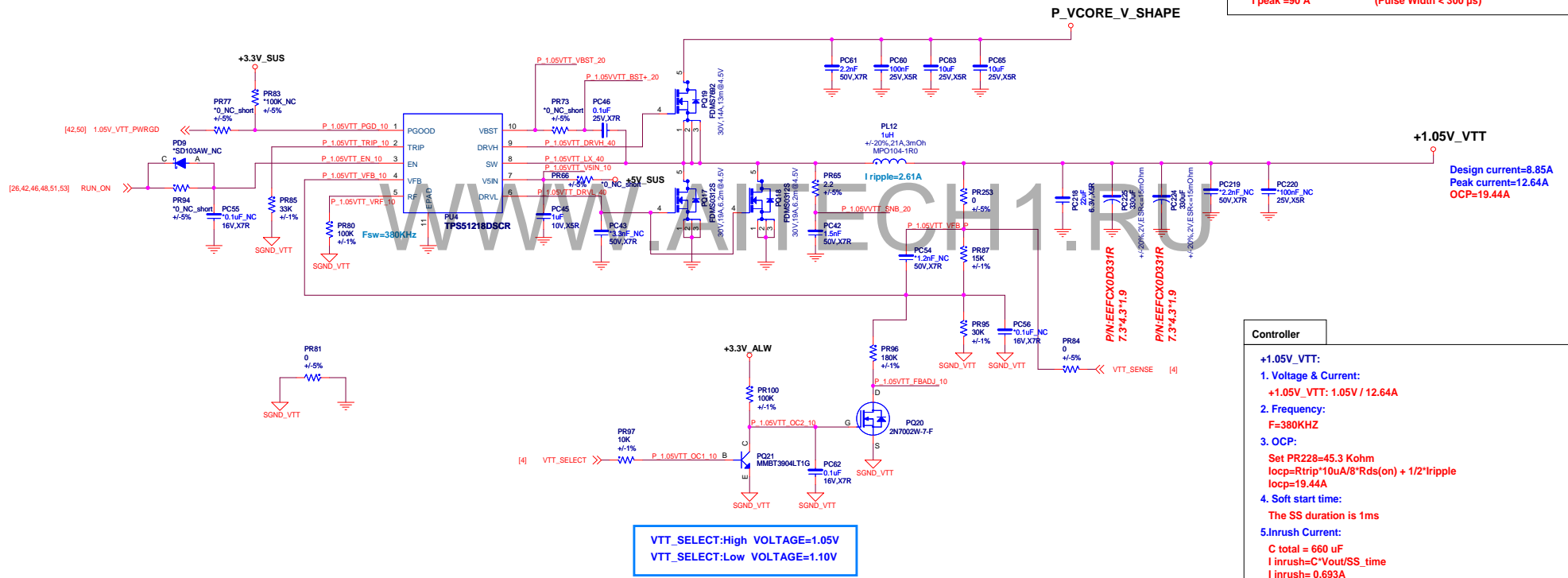
+NVDD:

1. Voltage & Current:  
+NVDD: 0.9V / 29A
2. Frequency:  
 $F = 300KHZ$
3. OCP:  
 $I_{ocp} = (OCP/2 - I_{ripple}/2) \cdot XDCR = 15mV$   
 $I_{ocp} = 40A$
4. Soft start time:  
The Soft Start duration is 1.25ms
5. Inrush Current:  
 $C_{total} = 990 \mu F$   
 $I_{inrush} = C \cdot V_{out}/SS_{time}$   
 $I_{inrush} = 0.7128A$

Power stage	
DDR III:	
1. I/P Current:	lin=Vo*Io/(0.75*Vin)=3.73A
2. Ripple Current:	Irip=3.45A
3. Ripple Voltage:	ESR/1=9mohm
	V=31.05mV
4. Inductor Spec:	
Isat=30A	
Idc=21A	
DCR=2.8mohm(Typ)	
5.MOSFET Spec:	
H-side MOSFET: FDMS7692	
Rds(ON)=9.5mohm(TYP)	(Vgs=4.5 V)
I cont = 14A	(T =25 °C)
I peak =50 A	(Pulse Width < 300 μs)
L-side MOSFET: FDMS0312S	
Rds(ON)=6.2mohm(Max)	(Vgs=4.5 V)
I cont = 19A	(T =25 °C)
I peak =90 A	(Pulse Width < 300 μs)



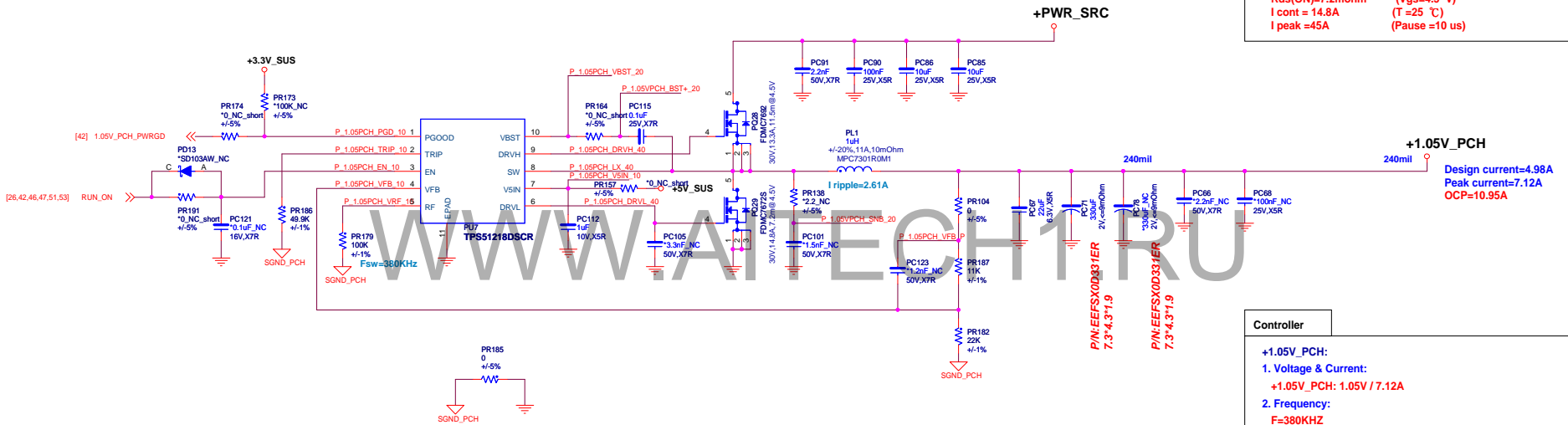
## +1.05V\_VTT POWER SUPPLY



Power stage	
<b>+1.05V_VTT:</b>	
1. <b>I/P Current:</b>	$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.97A$
2. <b>Ripple Current:</b>	$I_{rip} = 2.61A$
3. <b>Ripple Voltage:</b>	$ESR/2 = 7.5mohm$ $V = 19.575mV$
4. <b>Inductor Spec:</b>	$I_{sat} = 30A$ $I_{dc} = 21A$ $DCR = 2.8mohm$
5. <b>MOSFET Spec:</b>	H-side MOSFET: FDM57692
	$R_{ds(ON)} = 9.5mohm(TYP)$ ( $V_{gs} = 4.5V$ ) $I_{cont} = 14A$ ( $T = 25^\circ C$ ) $I_{peak} = 50A$ (Pulse Width < 300 $\mu s$ )
	L-side MOSFET: FDM50312S
	$R_{ds(ON)} = 6.2mohm(Max)$ ( $V_{gs} = 4.5V$ ) $I_{cont} = 19A$ ( $T = 25^\circ C$ ) $I_{peak} = 90A$ (Pulse Width < 300 $\mu s$ )

Controller	
<b>+1.05V_VTT:</b>	
1. <b>Voltage &amp; Current:</b>	<b>+1.05V_VTT: 1.05V / 12.64A</b>
2. <b>Frequency:</b>	<b>F=380KHZ</b>
3. <b>OCP:</b>	Set PR228=45.3 Kohm $I_{ocp} = R_{trip} \cdot I_{ouA} / 8 \cdot R_{ds(on)} + 1/2 \cdot I_{ripple}$ $I_{ocp} = 19.44A$
4. <b>Soft start time:</b>	The SS duration is 1ms
5. <b>Inrush Current:</b>	C total = 660 $\mu F$ $I_{inrush} = C \cdot V_{out} / SS\_time$ $I_{inrush} = 0.693A$

## +1.05V\_PCH POWER SUPPLY



## Power stage

**+1.05V\_PCH:**

- 1. I/P Current:**  
 $I_{in} = V_o / I_o (0.75 \times V_{in}) = 1.11A$   
**2. Ripple Current:**  
 $I_{rip} = 2.61A$   
**3. Ripple Voltage:**  
 $ESR / f = 9mohm$   
 $V = 23.49mV$   
**4. Inductor Spec:**  
 $I_{sat} = 23A$   
 $I_{dc} = 11A$   
 $DCR = 8mohm$   
**5. MOSFET Spec:**  
**H-side MOSFET: FDMC7692**  
 $R_{ds}(ON) = 11.5mohm$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 13.3A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 45A$  (Pause = 10 us)  
**L-side MOSFET: FDMC7672S**  
 $R_{ds}(ON) = 7.2mohm$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 14.8A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 45A$  (Pause = 10 us)

## Controller

**+1.05V\_PCH:**

1. **Voltage & Current:**  
+1.05V\_PCH: 1.05V / 7.12A
2. **Frequency:**  
F=380KHZ
3. **OCp:**  
Set PR184=56Kohm  
Iocp=RTrip\*(10uA/8\*Rds(on) + 1/2)\*ripple  
Iocp=10.95A
4. **Soft start time:**  
The SS duration is 1ms
5. **Inrush Current:**  
C total = 330 uF  
I inrush=C\*Vout/SS\_time  
I inrush= 0.3465A



## +5V\_ALW / +3.3V\_ALW POWER SUPPLY

### Power stage

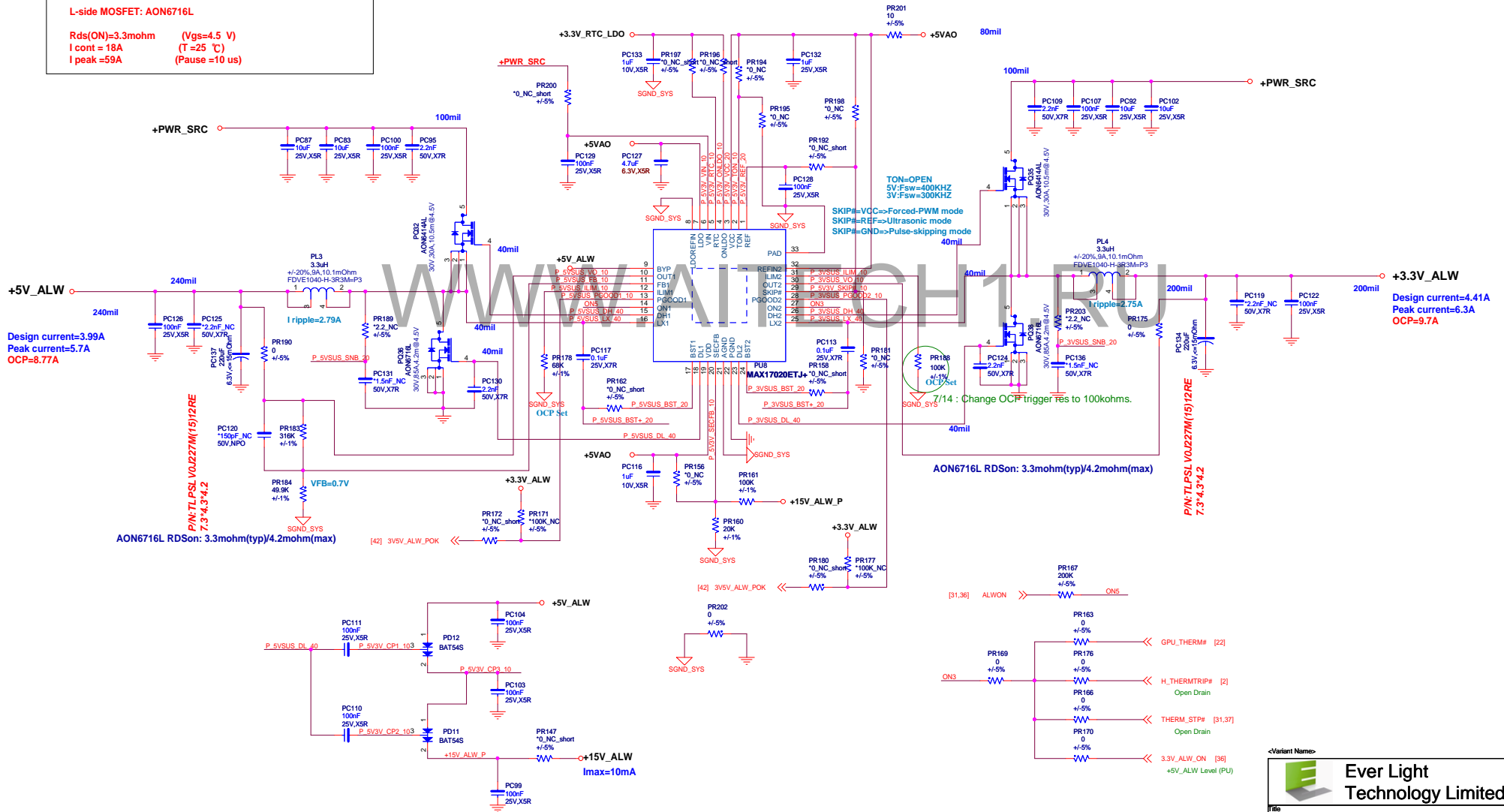
- +5V\_ALW:**
1. I/P Current:  
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 4.22A$
  2. Ripple Current:  
 $I_{rip} = 2.79A$
  3. Ripple Voltage:  
 $ESR/1 = 15m\Omega$   
 $V = 41.85mV$
  4. Inductor Spec:  
 $I_{sat} = 9.8A$   
 $I_{dc} = 9A$   
 $DCR = 10.1m\Omega$
  5. MOSFET Spec:  
H-side MOSFET: AON6414AL
- $R_{ds(ON)} = 30m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 13A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 27A$  (Pause = 10  $\mu s$ )

### L-side MOSFET: AON6716L

- $R_{ds(ON)} = 3.3m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 18A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 59A$  (Pause = 10  $\mu s$ )

### Controller

- +5V\_ALW:**
1. Voltage & Current:  
 $+5V\_ALW: 5V / 5.7A$
  2. Frequency:  
 $F = 400KHz$
  3. OCP:  
Set PR203=75 Kohm  
 $I_{ocp} = 5uA \cdot R_{ocp} / 10 \cdot R_{ds(on)}$   
 $I_{ocp} = 8.77A$
  4. Soft start time:  
The Soft Start duration is 1ms
  5. Inrush Current:  
 $C_{total} = 220 \mu F$   
 $I_{inrush} = C \cdot V_{out} / SS\_time$   
 $I_{inrush} = 1.1A$
- +3.3V\_ALW:**
1. Voltage & Current:  
 $+3.3V\_ALW: 3.3V / 6.3A$
  2. Frequency:  
 $F = 300KHz$
  3. OCP:  
Set PR211=82Kohm  
 $I_{ocp} = 5uA \cdot R_{ocp} / 10 \cdot R_{ds(on)}$   
 $I_{ocp} = 9.7A$
  4. Inrush Current:  
 $C_{total} = 220 \mu F$   
 $I_{inrush} = C \cdot V_{out} / SS\_time$   
 $I_{inrush} = 0.726A$



<Variant Name>

**Ever Light Technology Limited**

49 - PW\_SYSTEM(MAX17020)

Size Document Number  
Nichols 14". SW\_Ard\_Eric Ho

Date: Friday, August 20, 2010 Sheet 49 of 59

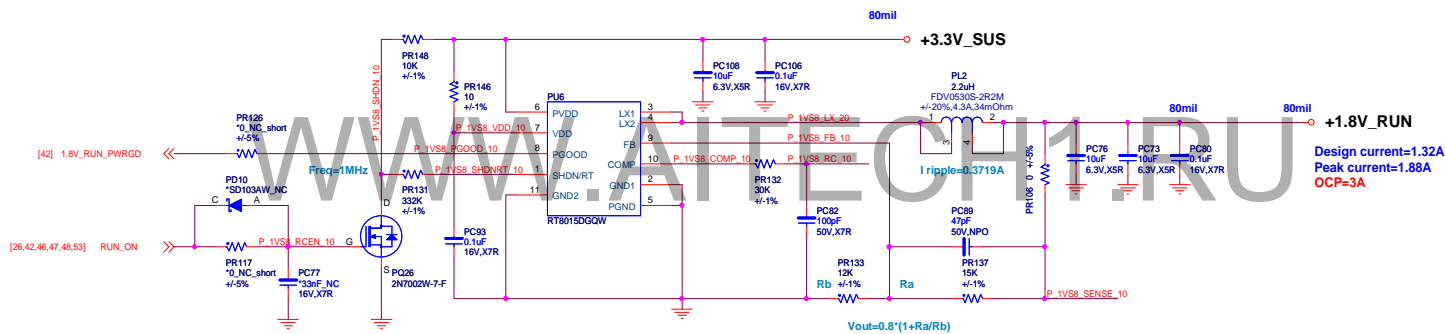
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Ever Light  
Technology Limited

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Date			Rev
Friday, August 20, 2010			1A
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## +1.8V\_RUN POWER SUPPLY



+1.8V\_RUN @ 2A

### 1. Supply Voltage:

**VIN = 3.3V (2.6V ~ 5.5V)**

## 2. Supply Voltage:

**VOUT = 1.8V / 2A**

### 3. Current Limit:

**I limit =3.2A(min)/3.8A(Typ)**

#### 4. Continue Current:

**I cont = 2A**

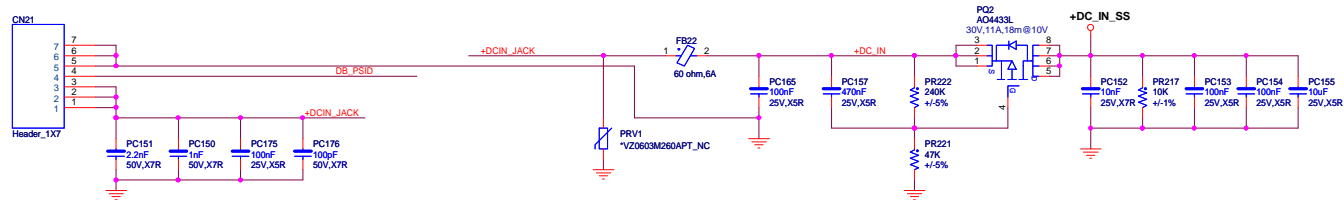
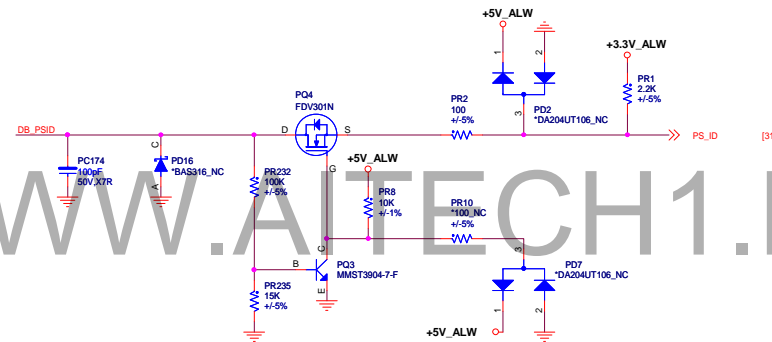
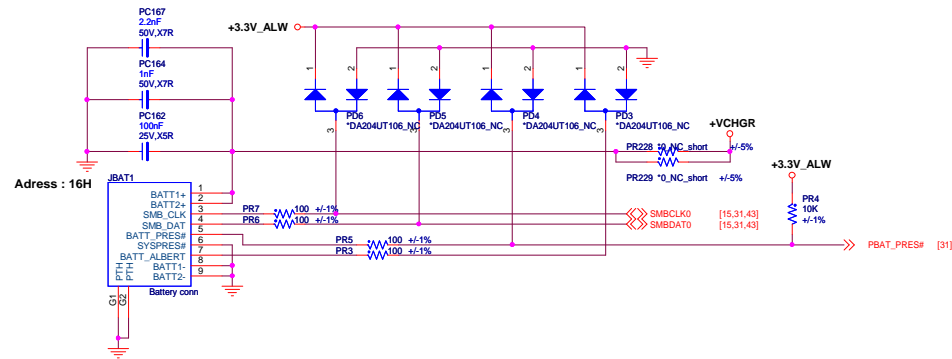
### 5. Feedback Voltage:

**VFB = 0.8V**

### 6. Switching Frequency:

**Rrt = 332 Kohm**

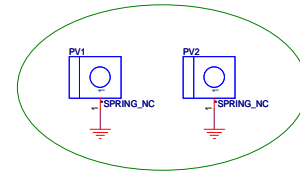
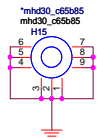
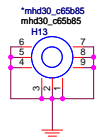
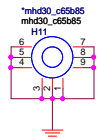
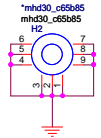
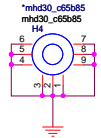
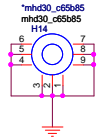
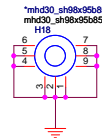
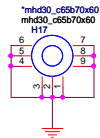
**Fsw = 1000 KHz**



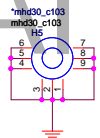
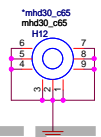
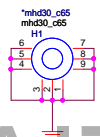
<Variant Name>





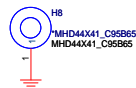
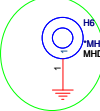


C114 4/14: Add touch panel power switch per N-Trig recommended.

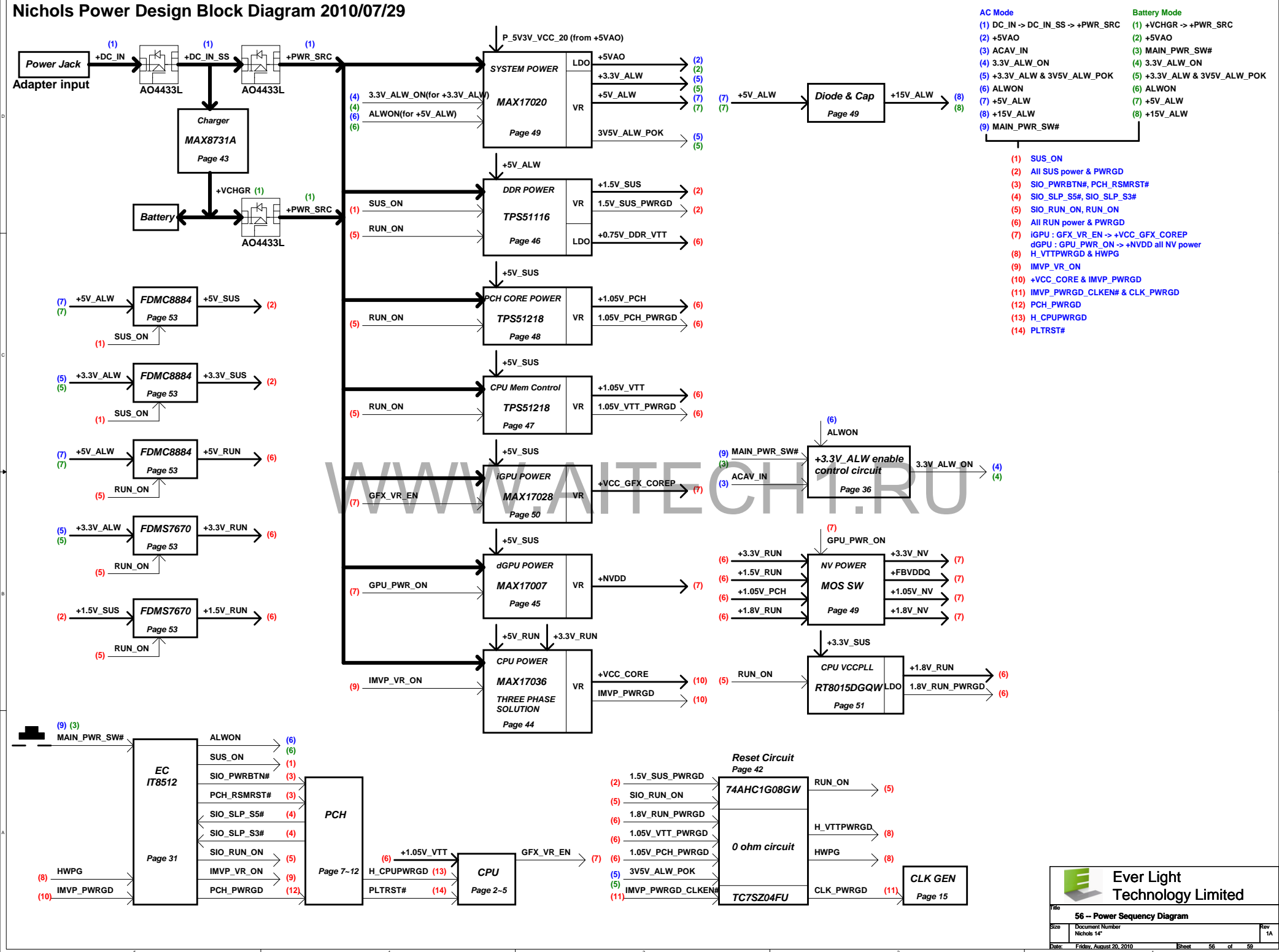


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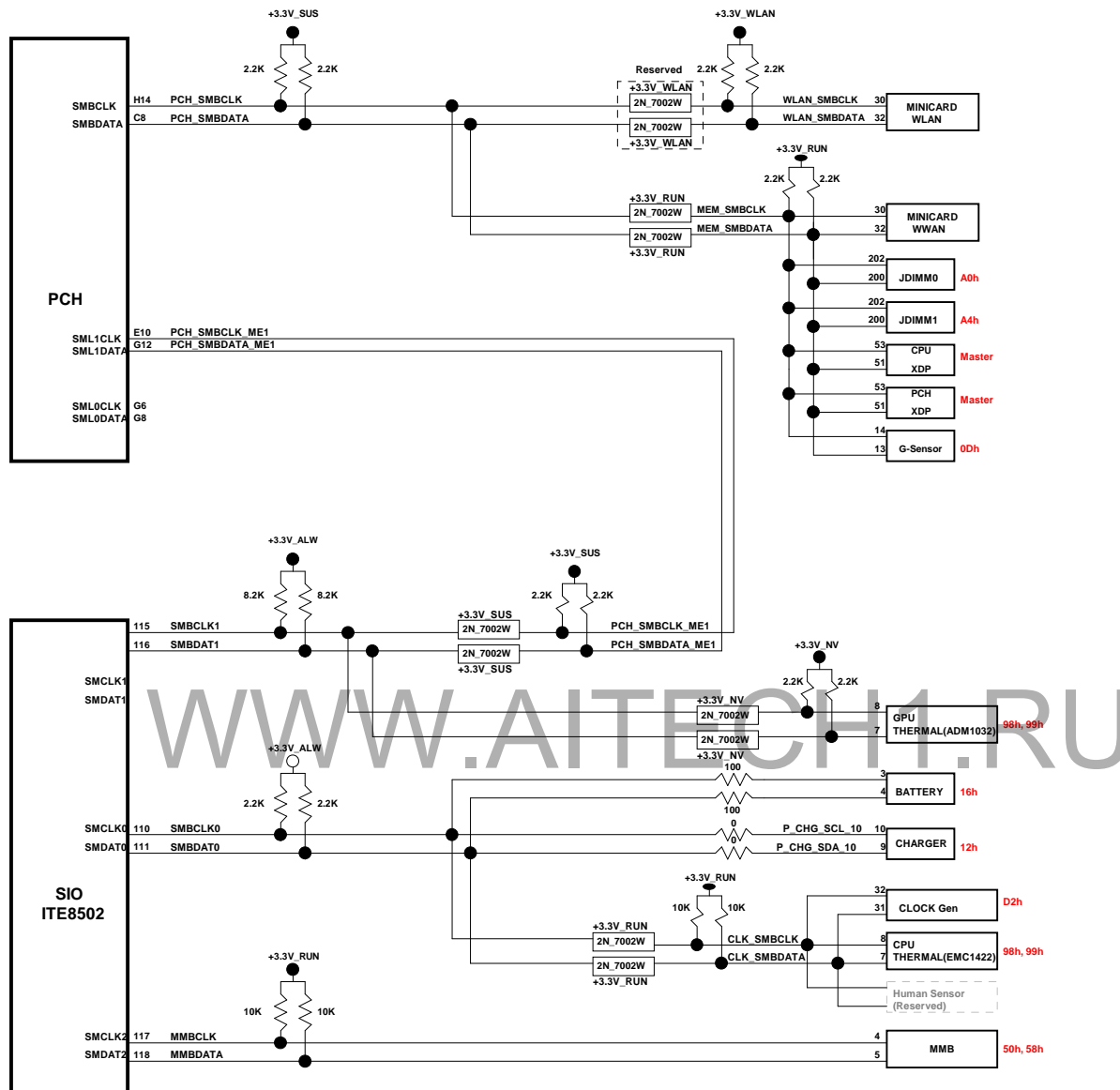
3/12 Hank: Add back H6 .and delete H16



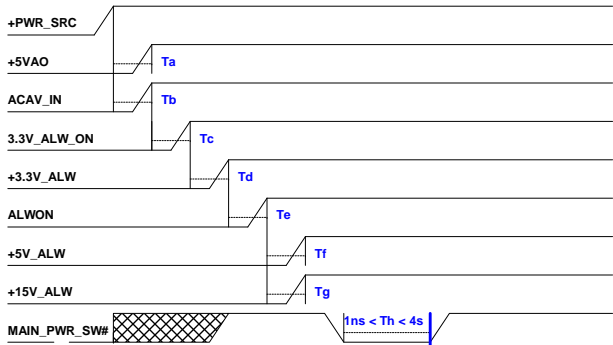
## Nichols Power Design Block Diagram 2010/07/29



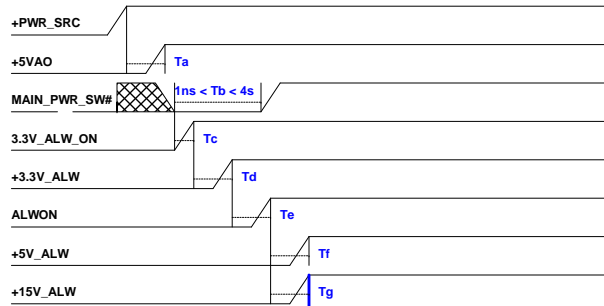




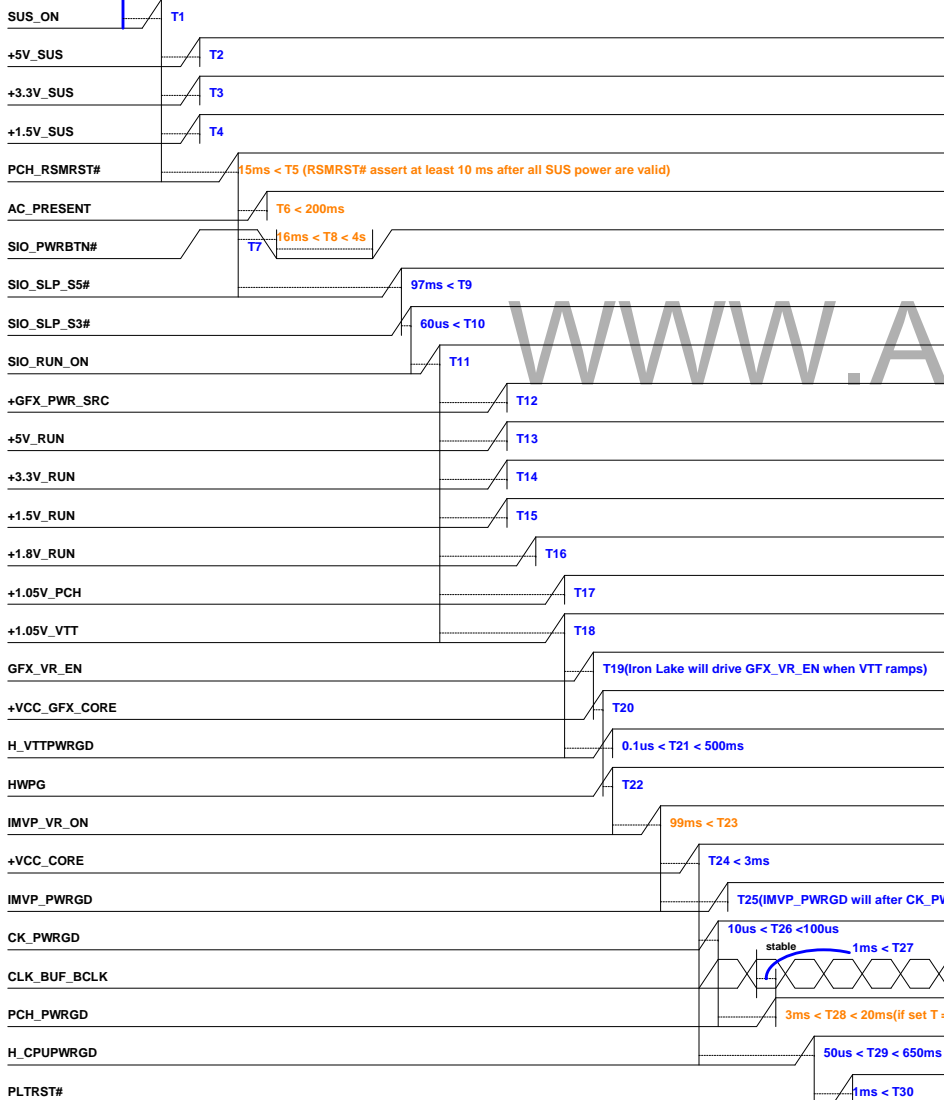
## [AC with USB charge]



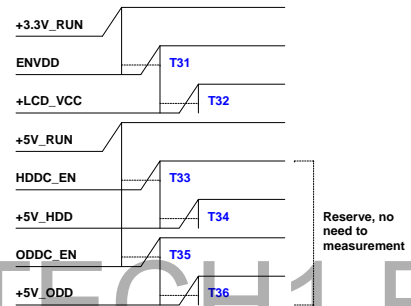
## [Battery without USB charge]



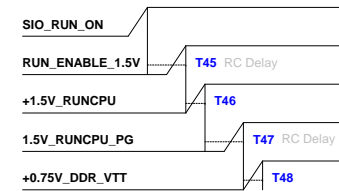
EC pay attention timing



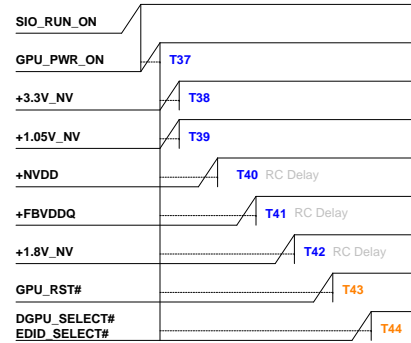
## [LCD, HDD and ODD Power Sequence]



## [W/ S3 Power Reduction DDR3 Sequence]



## [GPU Power Sequence]



The ramp up time for any rail must be more than 40us.

+NVDD <= +3.3V\_NV + 0.5V

+FBVDDQ <= +3.3V\_NV + 0.5V

GPU\_RST# must de-asserted after all power rails reach within it's spec.  
DGPU\_SELECT# and EDID\_SELECT# must get set after GPU\_RST#

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
MBB	1	49	7/14				+3.3V_ALW current will over OCP design point.	Change PR188 to 100kohms.
	2	10	7/14				+3.3V_RUN will have a leakage via WWAN card from WWAN_RADIO_DIS# PU.	NC R436.
	3	22	7/14				Change FB23 from DCR 100m ohms to 50m ohms per NV recommand.	Done.
	4	31	7/14				1. Change BID to ST2 stage setting. 2. Change Config ID RES from 5% to 1% per using wrong part.	Change R545 to 33Kohms. Done.
	5	10	7/14				WWAN card cannot be recgnized when system wake up from S3.	Change WWAN_RADIO_DIS# PCH GPIO from GPIO15 to GPIO35.Delete R437.
	6	26	7/20				Change N-Trig digitizer power plan from RUN to SUS for supporting fast wake up feature.	NC R808 and pop R809.
	7	26	7/20				Remove U3, R784 and pop R59 for PWM only from EC.	Done.
	8		7/26				SMT request	Change L1,L4,L6,L22,L23 footprint from cks0805h11 to cks0805h13.
	9	10,26	7/27				Solve GPIO glitch issue	Change P26 net USB_OC2# to LPM#,R796 0 ohm change to 100 ohm,P10 GPIO15 change to LPM#
	10	08,31	7/27				Change by PUR request	Change X4,Y1 PN to 710104400-310-G,footprint to x4s69x14h14
	11		7/28				Remove 0ohm resistor for ST2 stage	Modify as excel file"Nichols_0 ohm removal list(ST2)_0728_Scott"
	12	55	7/28				Modify screw hole type for MP	Change H17,H18,H14,H4,H2,H11,H13,H15,H1,H12,H5 footprint.
	13	18,19	7/29				Layout request	Change VRAM U1,U2,U5,U10,U37,U38,U41,U43 footprint to fbga96gh12_MBB
	14	56	7/29				Power diagram update	Change P56 for power diagram update
	15	49,46	7/30				Power fine tune OCP resistors value	Change PR188 to 100K,PR178 to 68K,PR215 to 6.3K.
	16	34	8/2				Fine tune LED brightness	Change P699 330ohm to 470ohm
	17	21,44,45	8/3				Reserved Ventura function	NC for Q44,Q45,R680,R678,PC247,PC248,PR216,PR292, PR288,PC234,PU12,PR289,PR290,PR239,PR33, PR36,PC22,PU1,PR37,PR38,PC184,PC183
	18		8/3				PN category issue	Change C417,C746,PC71,PC78,PC187,PC188,PC193 PN from 62110DD00-024-G to 62120B000-024-G
	19	26	8/3				Fine tune N-TRIG resistor value	Change R796 tolerance from +/-5% to +/-1%.
	20	24	8/4				Fine tune HDMI_TX2+_BOUT/HDMI_TX2-_BOUT signal eyes.	Change R162 to 383ohm
	21	26	8/16				Fine tune N-TRIG timing to meet SPEC(100ms)	Change GPIO15 to GPIO41
	22	31	8/16				BIOS setting strap for BID	Change R545 to 100Kohm
	23		8/20				Remove power portion 0 ohm for X-build	Modify as excel file"Nichols_0 ohm removal list(A00)_Scott"
								 <div> <div>Ever Light Technology Limited</div> <div> <div>Title</div> <div>59 – Change list-2</div> </div> <div> <div>Size</div> <div>Document Number</div> <div>Nichols Discrete</div> <div>Rev</div> <div>1A</div> </div> <div> <div>Date:</div> <div>Friday, August 20, 2010</div> <div>Sheet</div> <div>59</div> <div>of</div> <div>59</div> </div> </div>